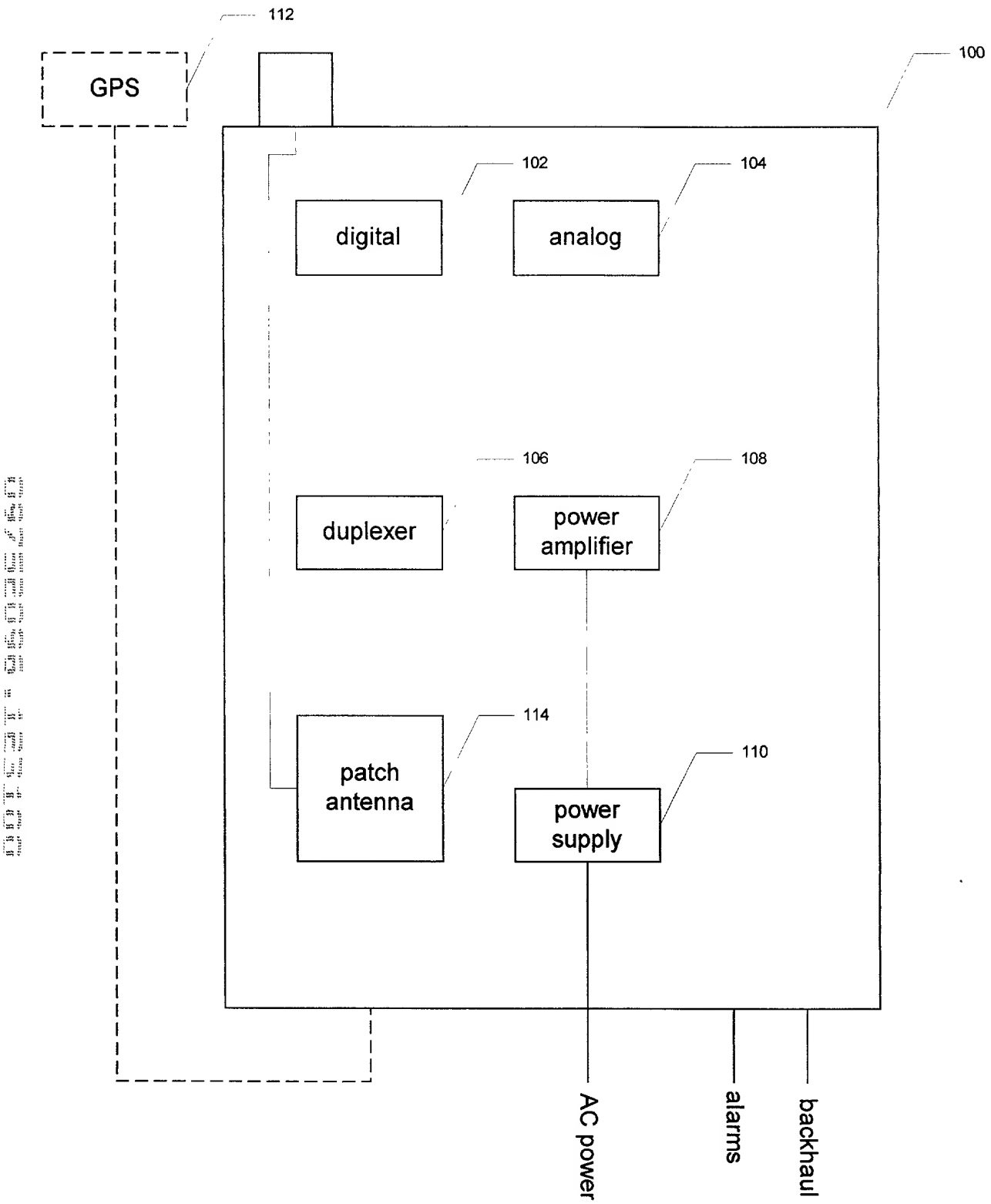
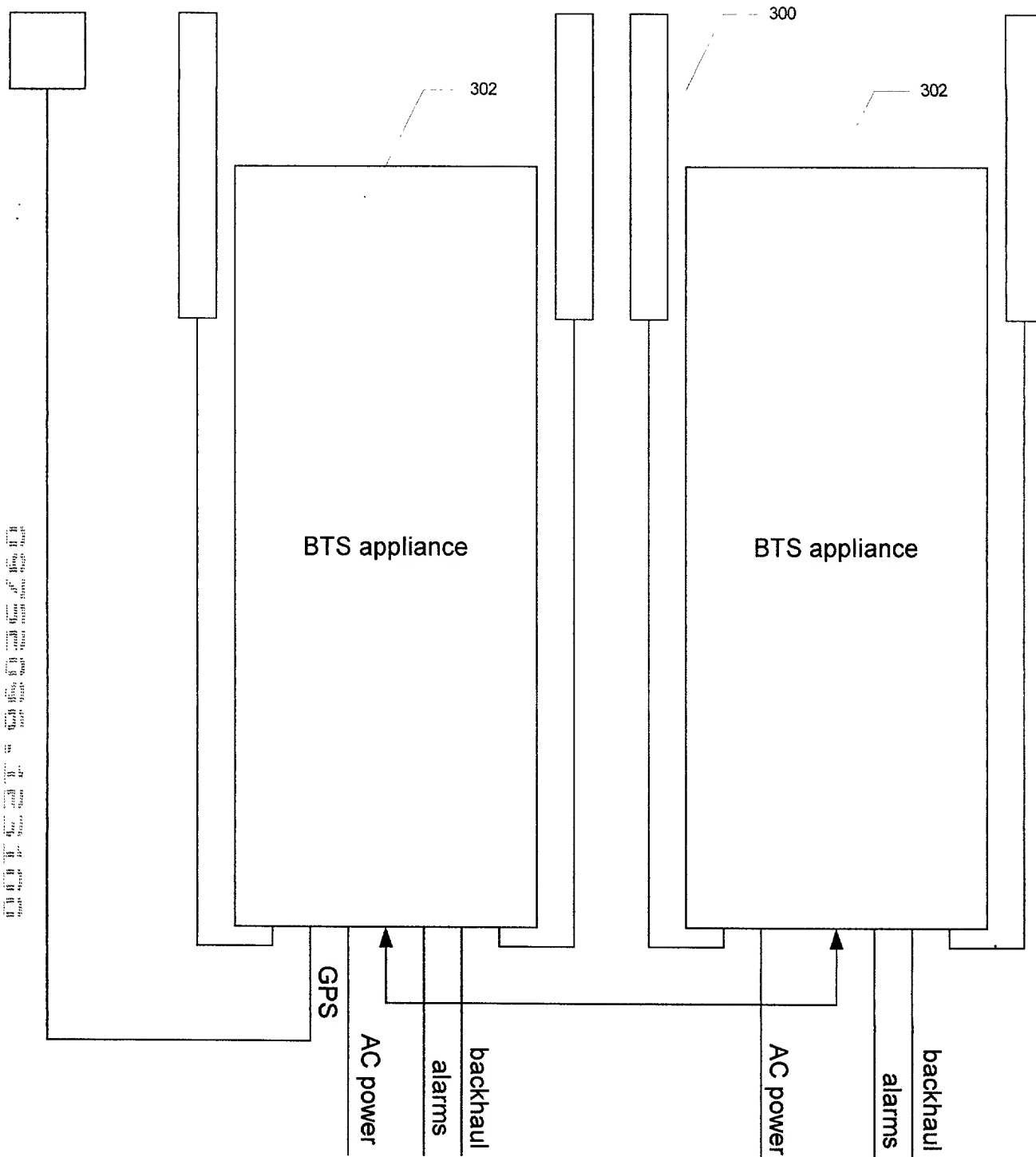


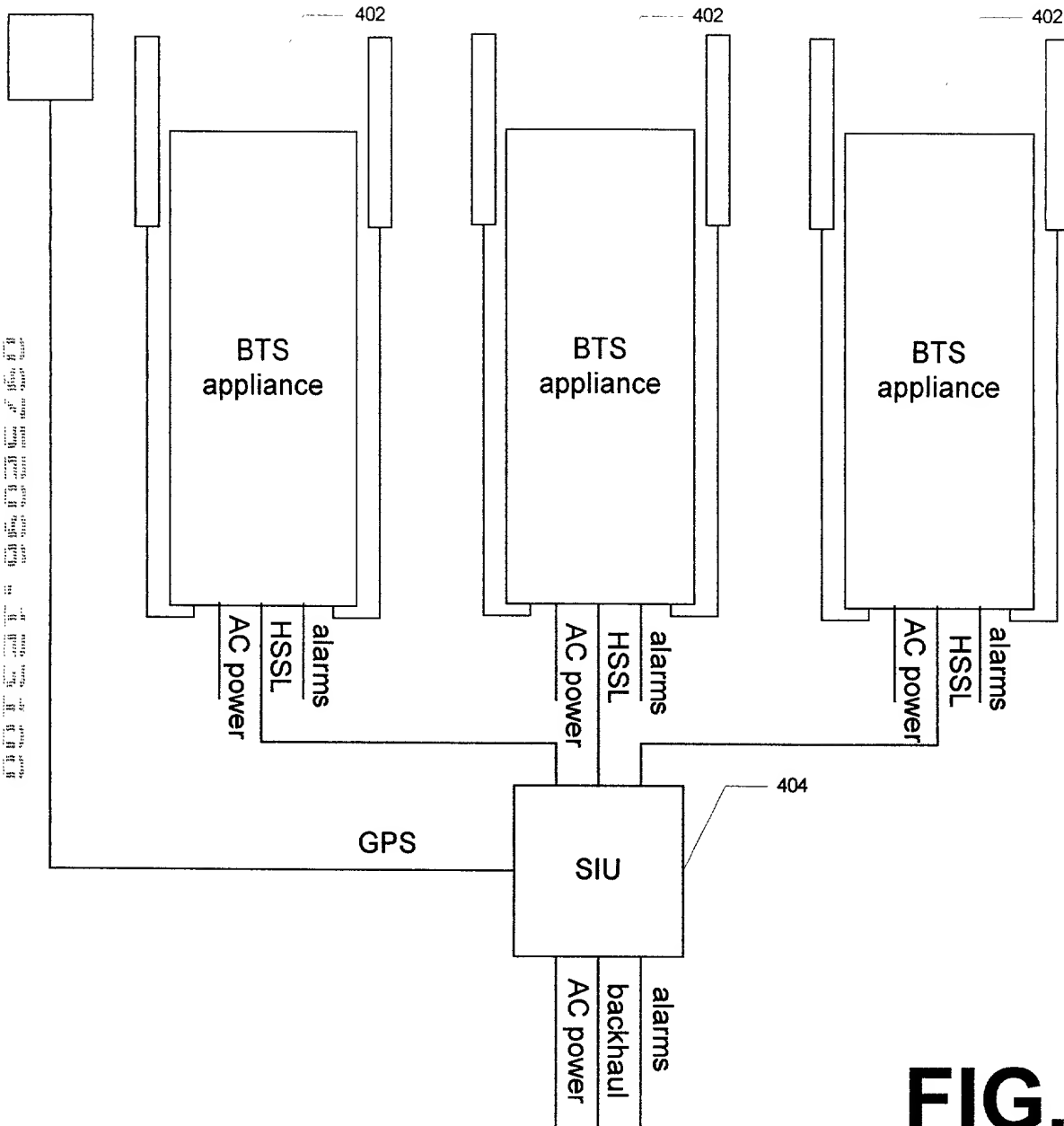
**FIG. 1**



**FIG. 2**



**FIG. 3**



**FIG. 4**

FIG. 5 is a block diagram of a system architecture for a network of Base Transceiver Stations (BTS) connected to a central System Integration Unit (SIU).

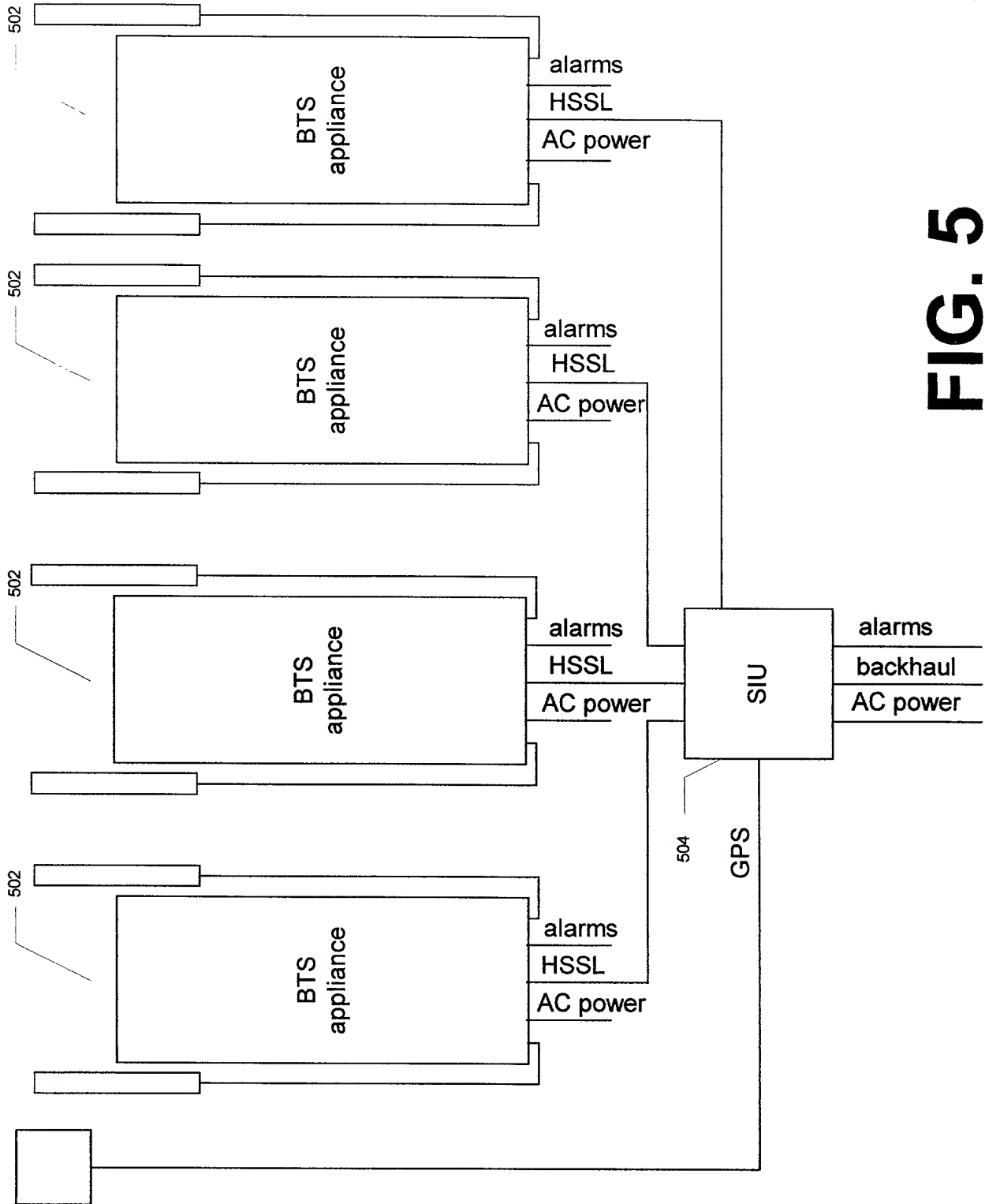


FIG. 5



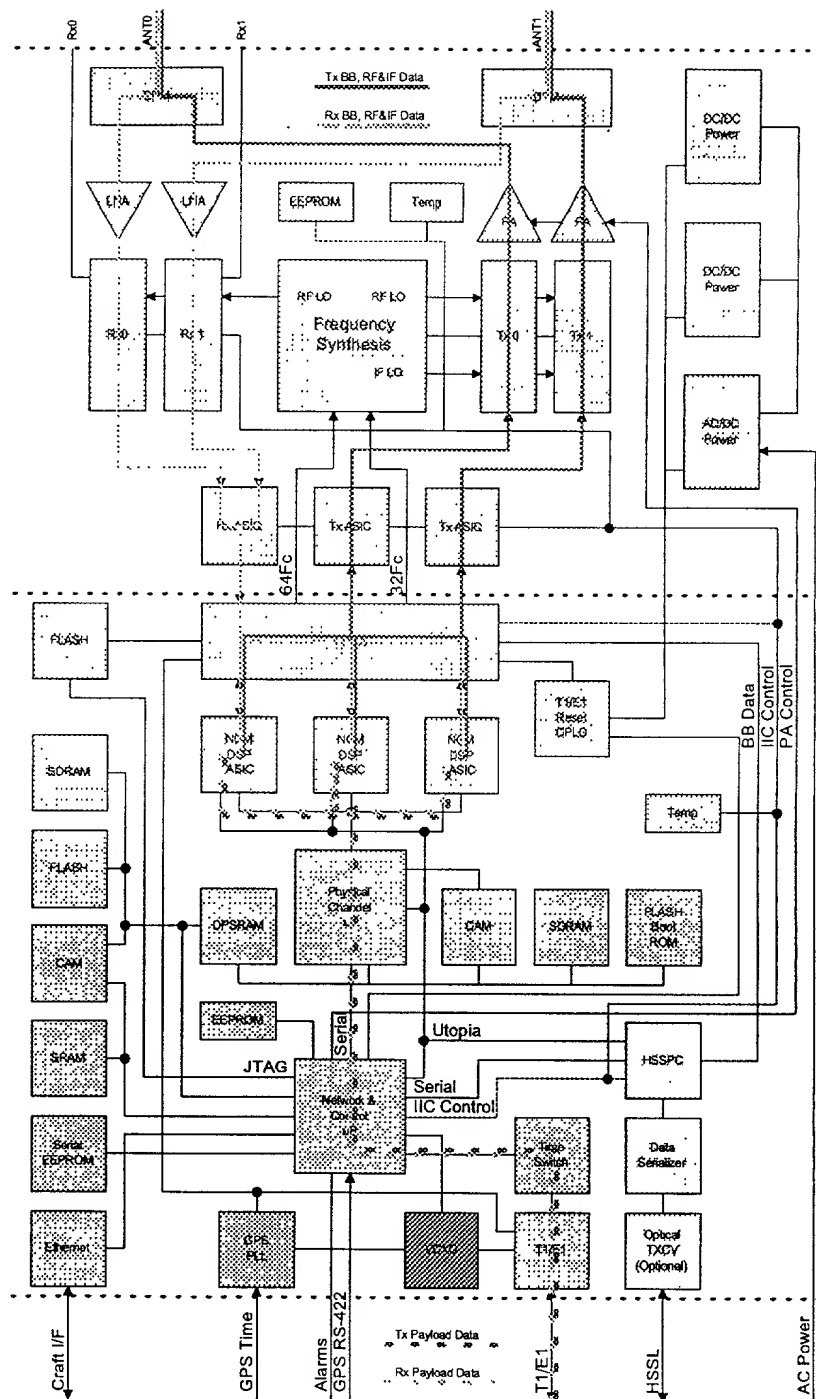


FIG. 7

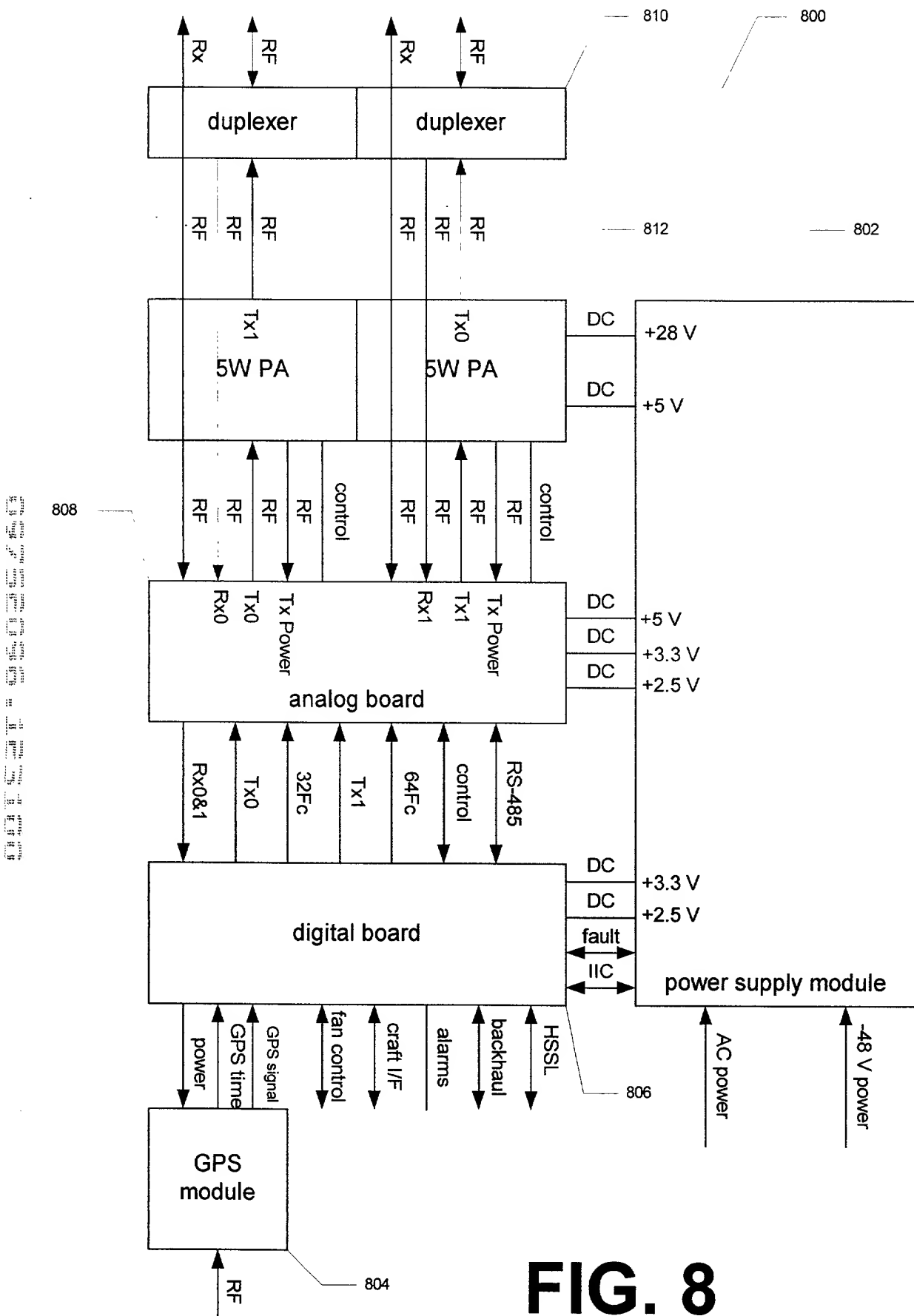
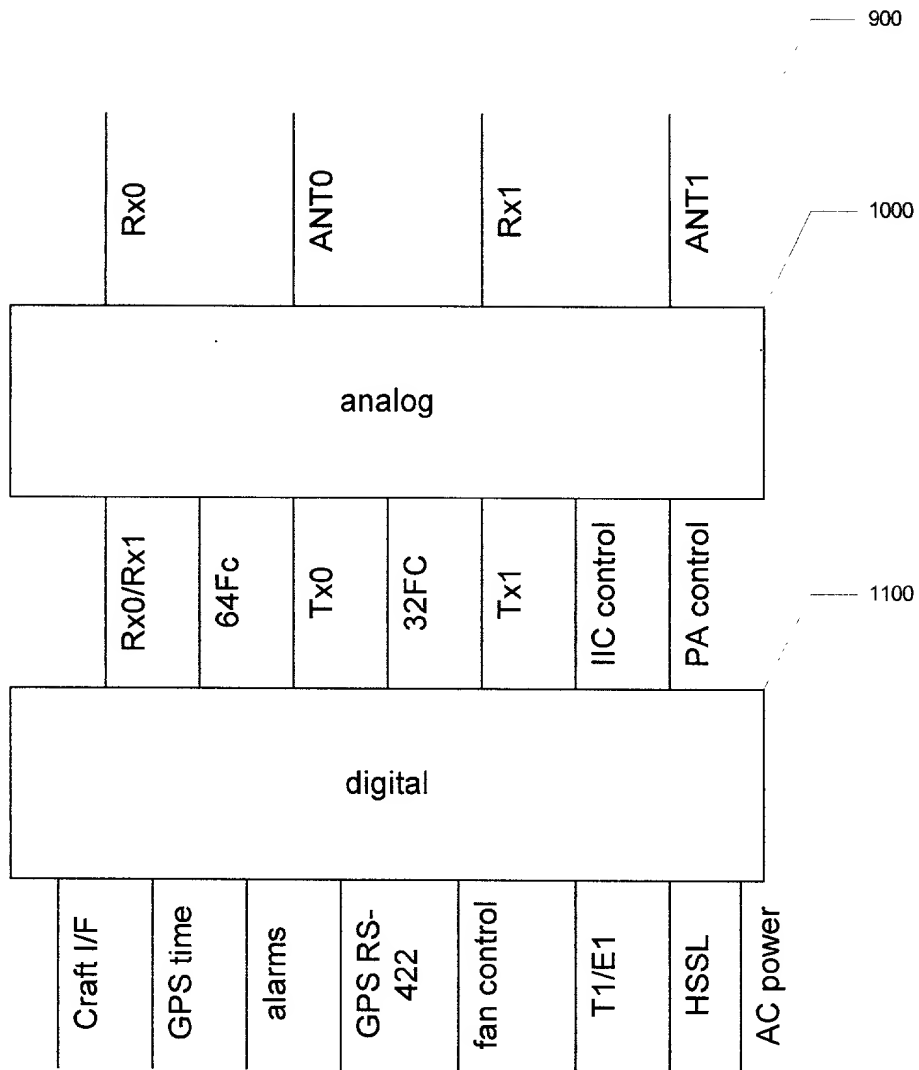


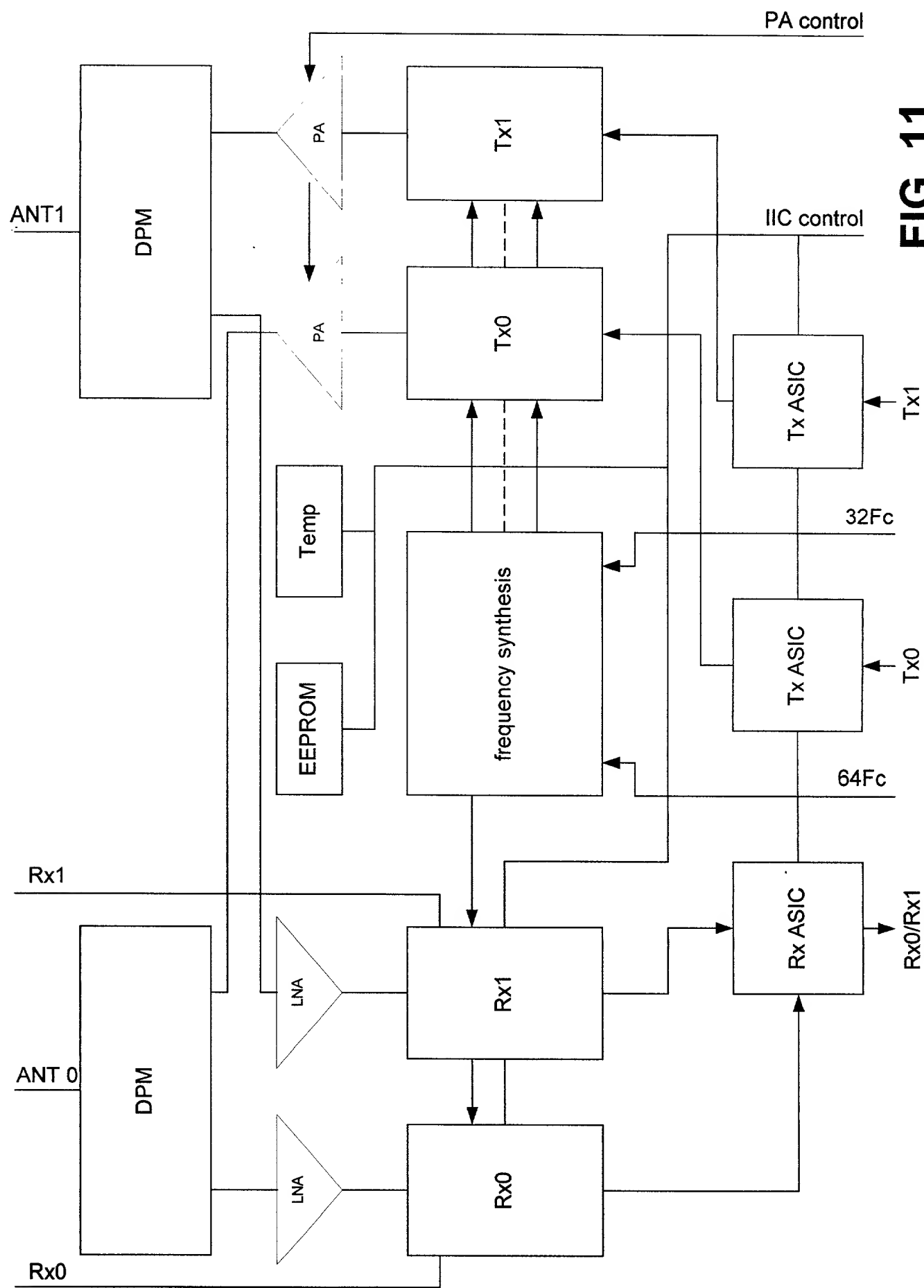


FIG. 9 is a block diagram of a system 900, which includes a digital block 1100 and an analog block 1000. The digital block 1100 includes a Craft I/F, GPS time, alarms, GPS RS-422, fan control, T1/E1, HSSL, and AC power. The analog block 1000 includes Rx0/Rx1, 64Fc, Tx0, 32Fc, Tx1, IIC control, and PA control. The system 900 also includes Rx0, ANT0, Rx1, and ANT1.

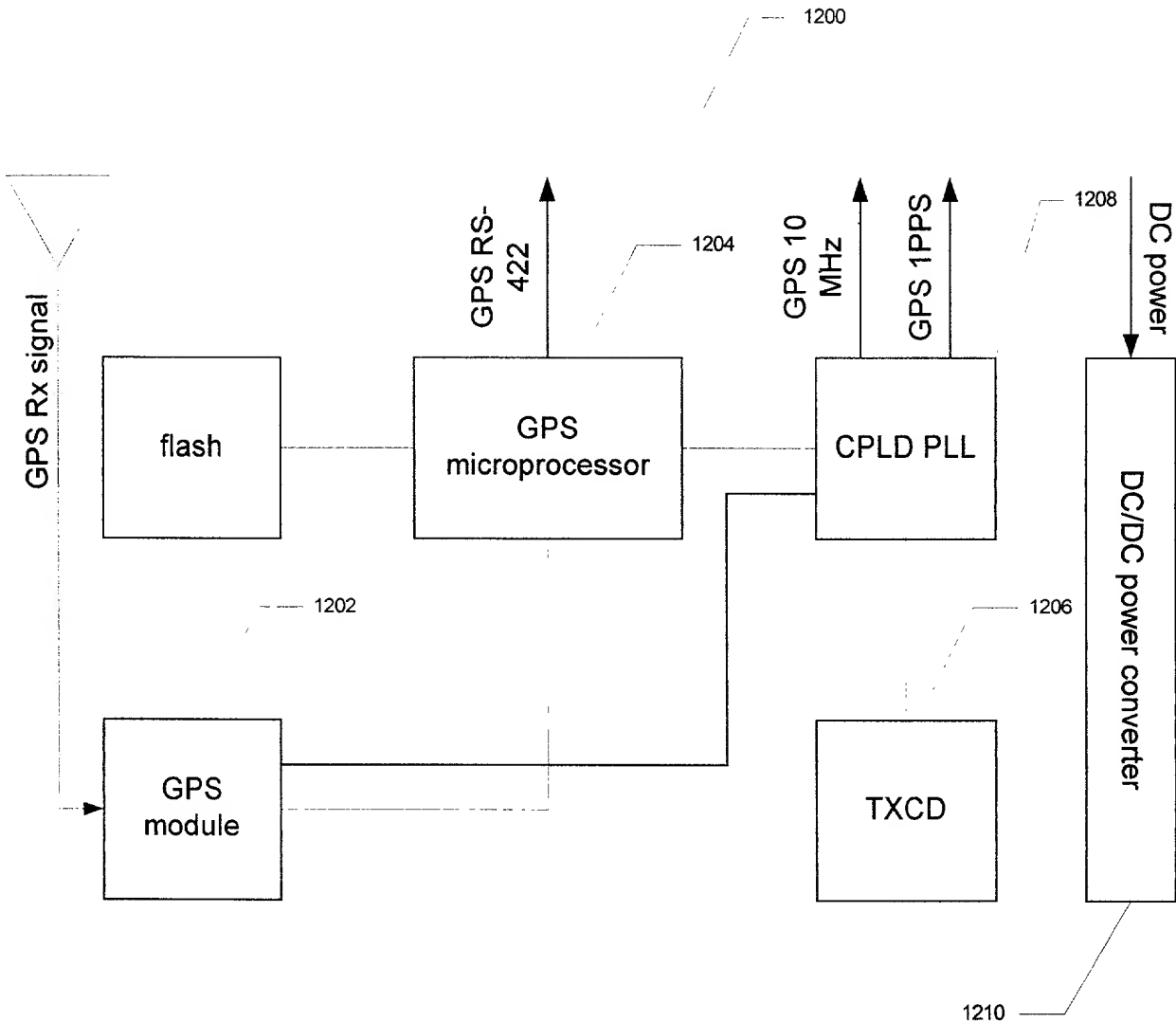


**FIG. 9**

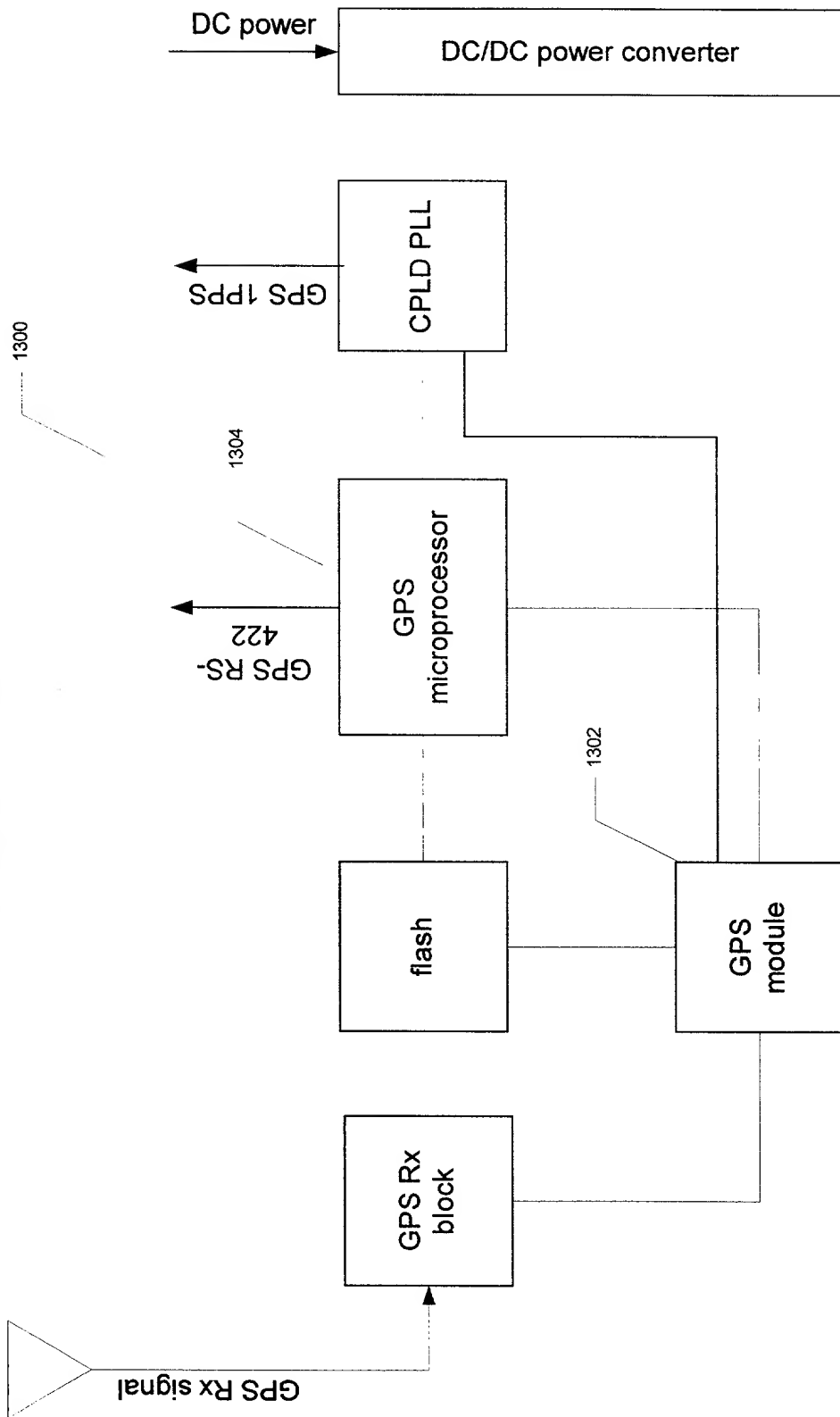




**FIG. 11**



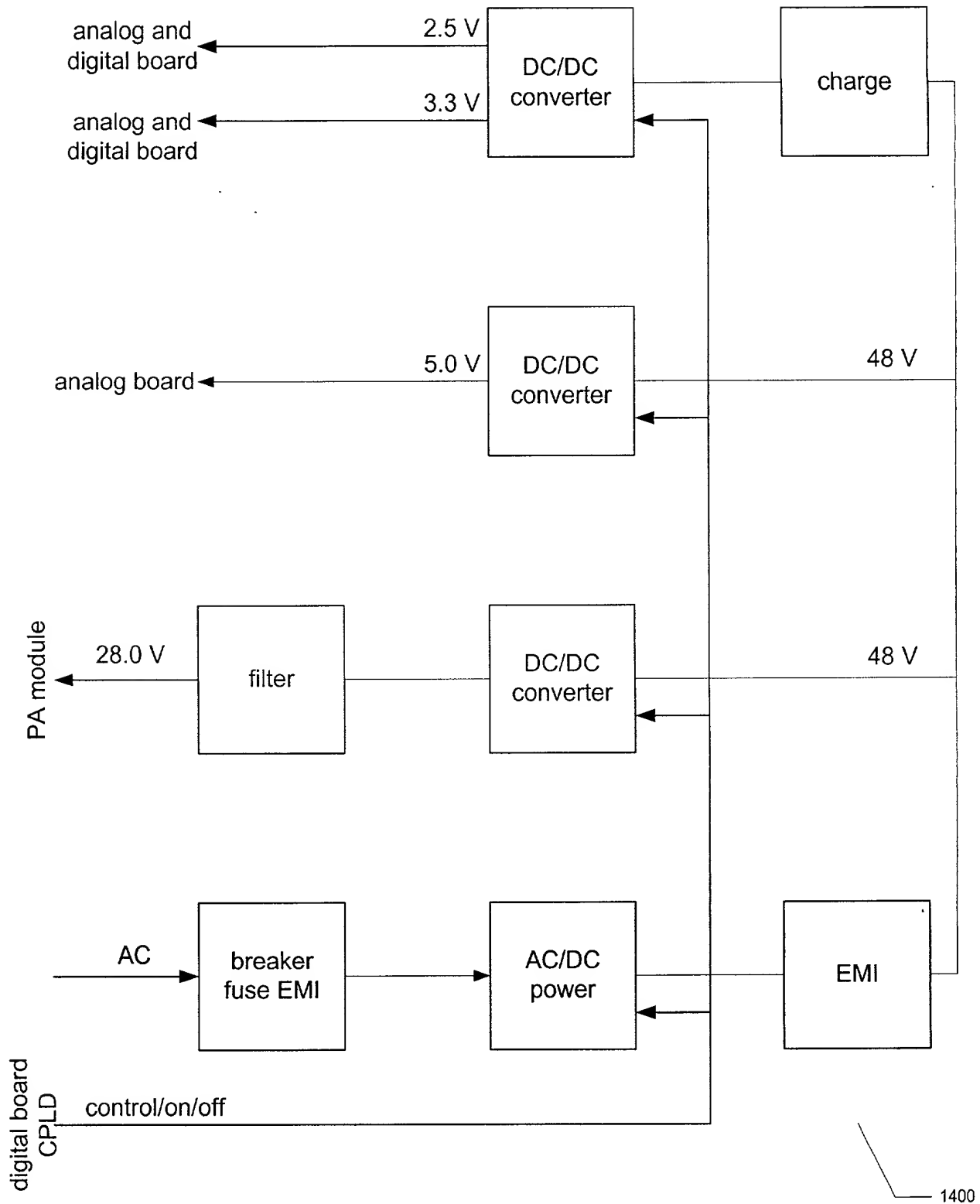
**FIG. 12**



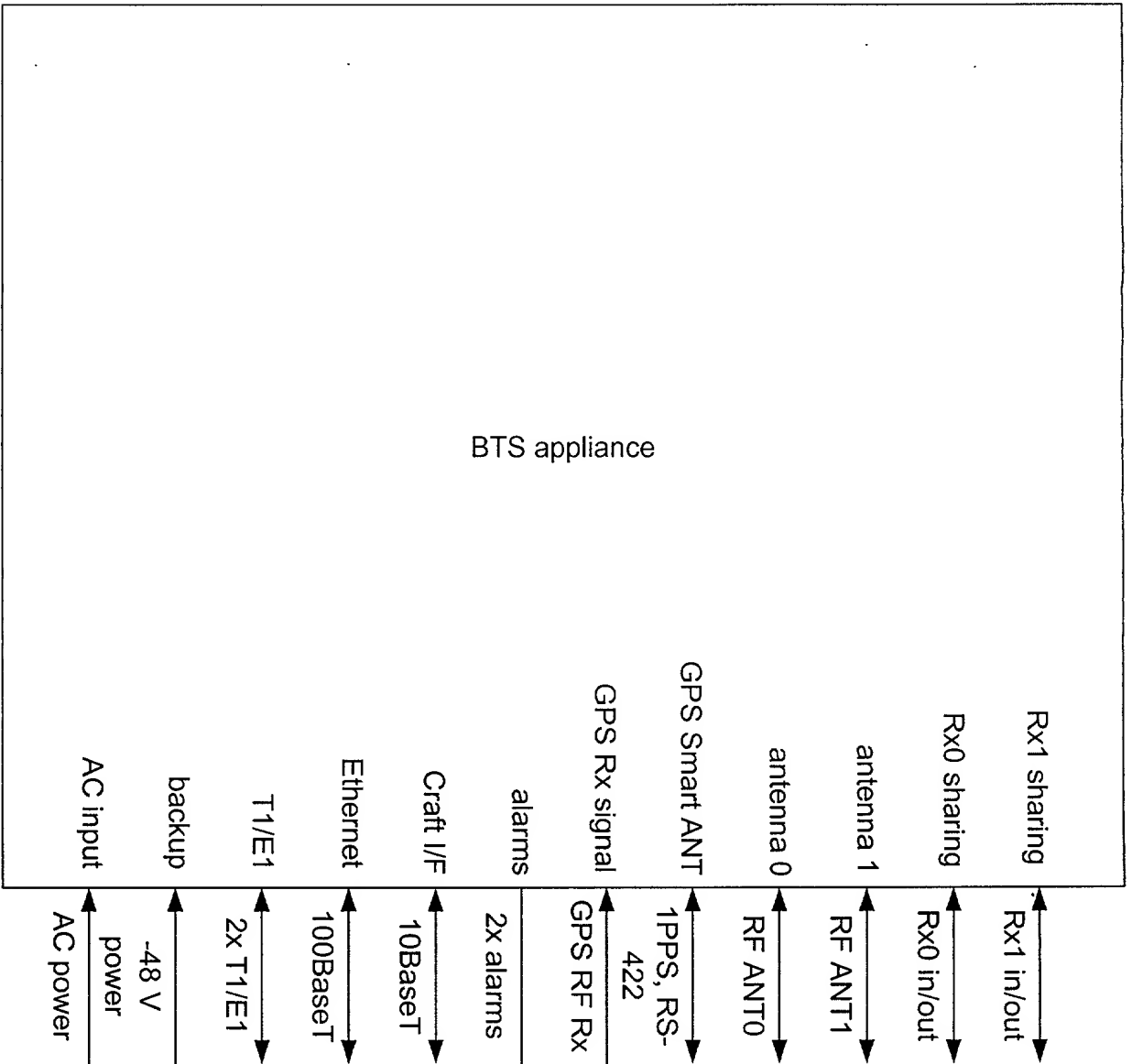
1306

FIG. 13

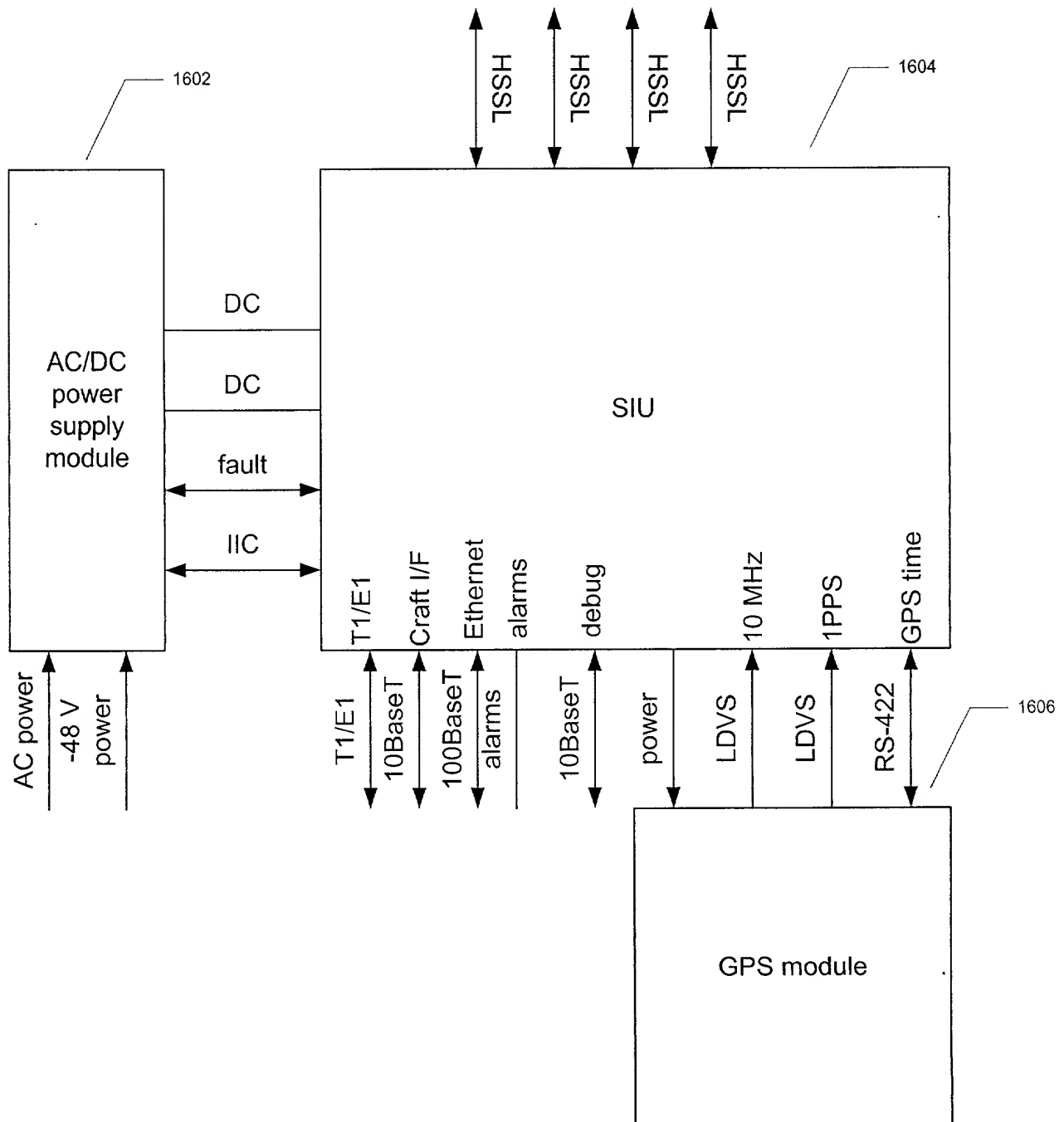
FIG. 14 is a block diagram of a power supply system 1400. The system includes an AC input, a breaker fuse EMI, an AC/DC power converter, a DC/DC converter, a filter, a PA module, a digital board CPLD, a charge controller, and an EMI filter. The AC input is connected to the breaker fuse EMI, which is connected to the AC/DC power converter. The AC/DC power converter outputs 48 V to the DC/DC converter and the EMI filter. The DC/DC converter outputs 2.5 V and 3.3 V to the analog and digital board, and 5.0 V to the analog board. The DC/DC converter is connected to the filter, which outputs 28.0 V to the PA module. The digital board CPLD is connected to the DC/DC converter and the AC/DC power converter. The charge controller is connected to the DC/DC converter and the EMI filter. The EMI filter is connected to the AC/DC power converter and the DC/DC converter.



**FIG. 14**



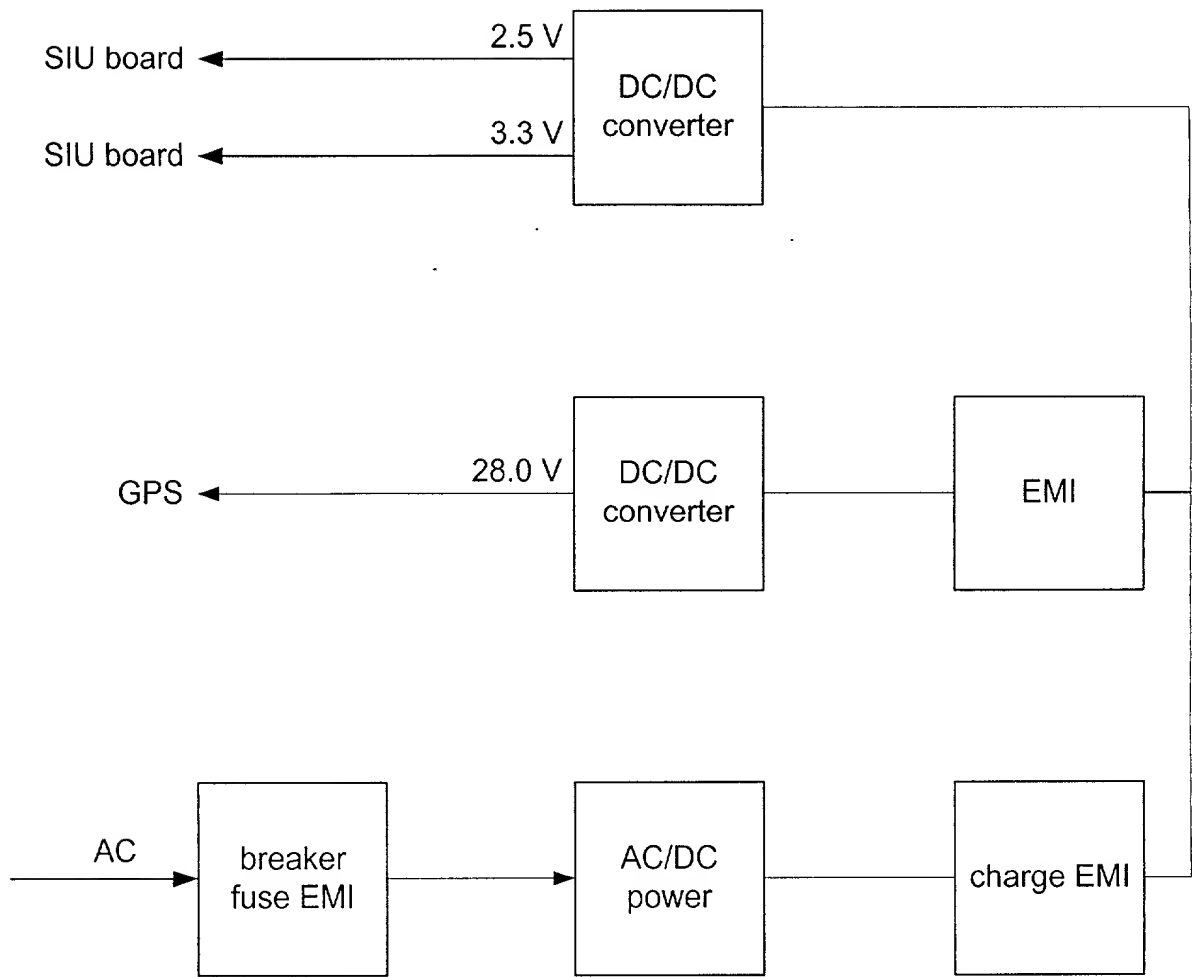
**FIG. 15**



**FIG. 16**

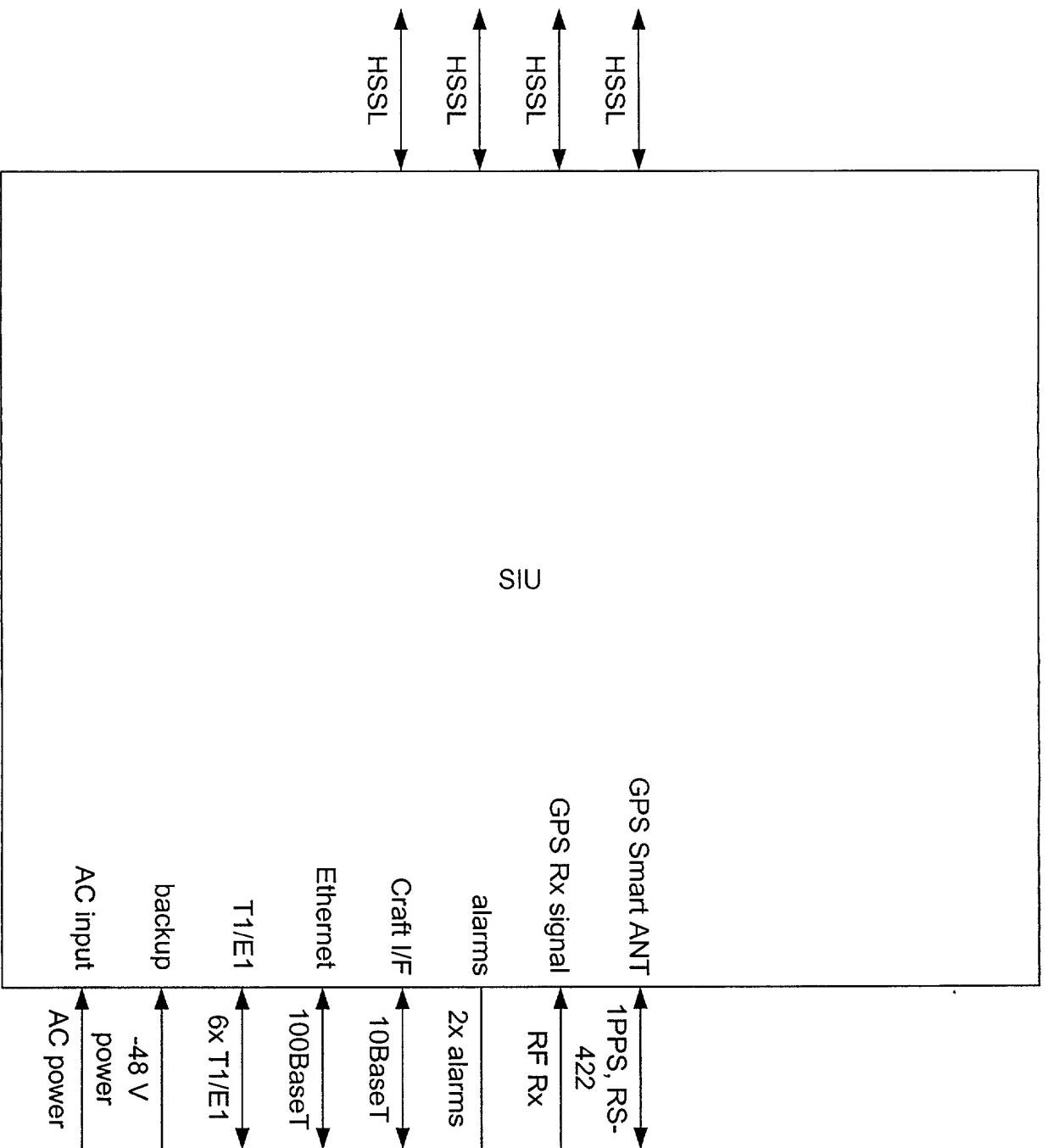






1602

**FIG. 18**



**FIG. 19**

FIG. 20 is a block diagram of a system architecture. The diagram is divided into three main sections: a top section for RF and baseband processing, a middle section for system control and data processing, and a bottom section for external interfaces and power management.

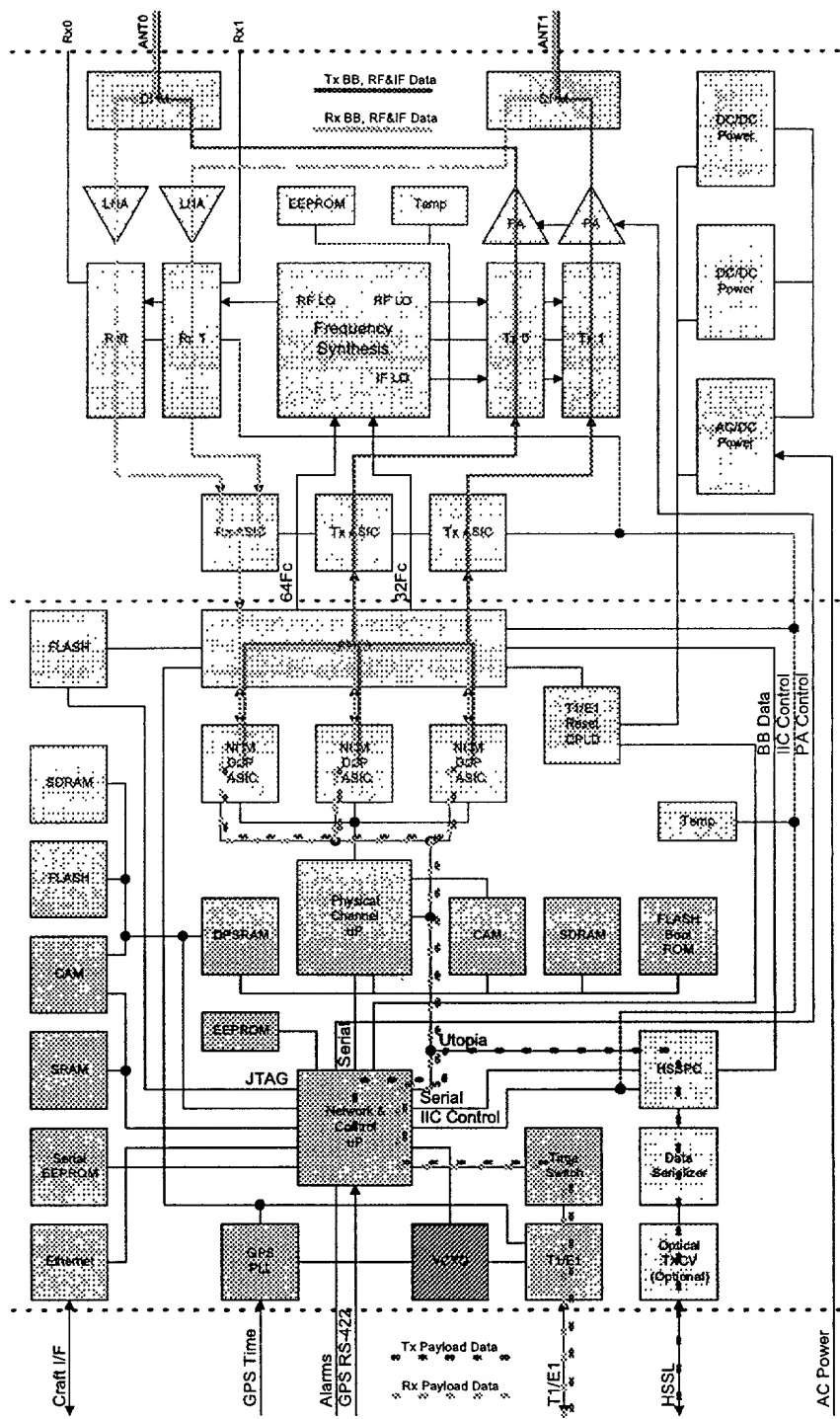
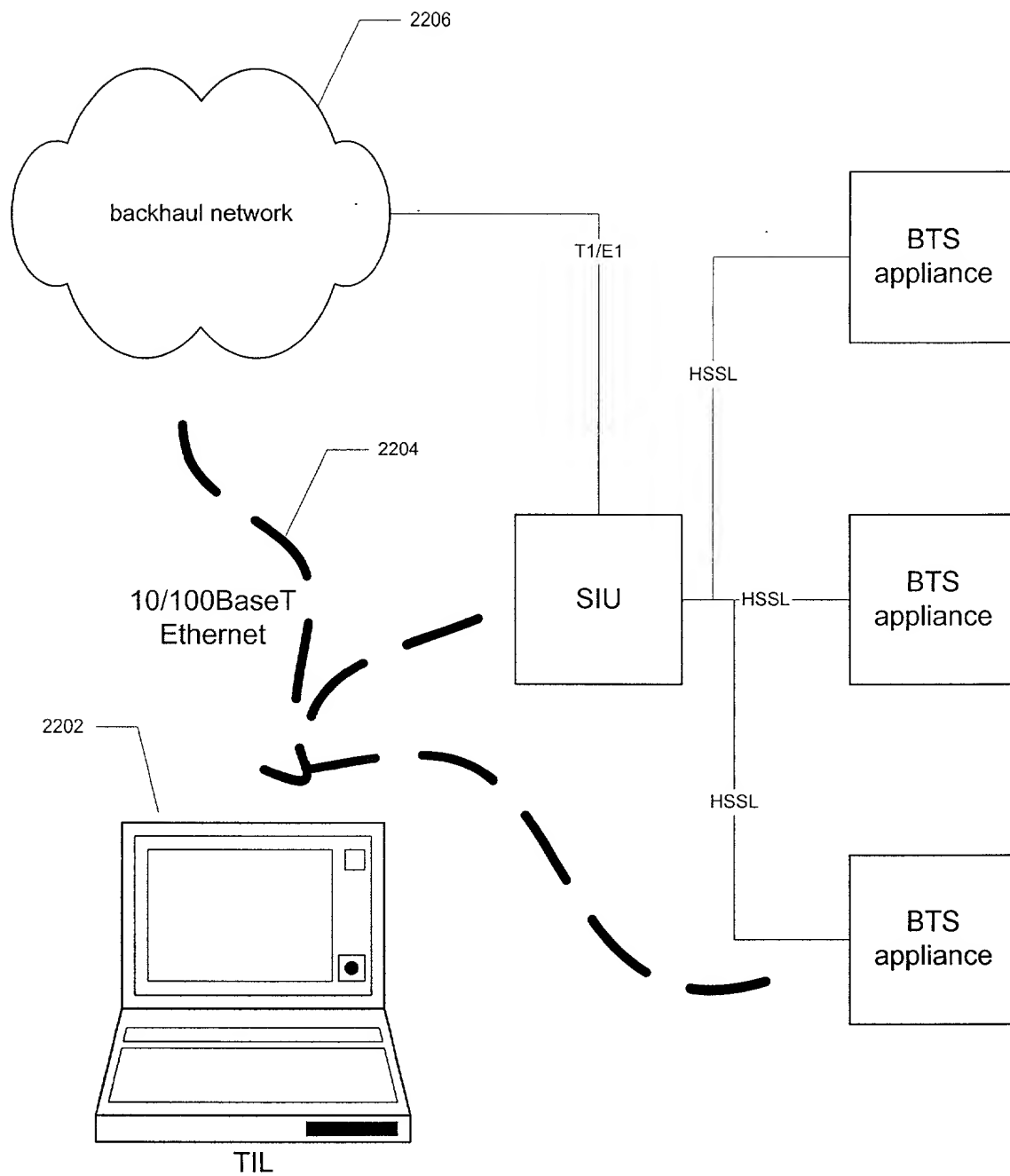


FIG. 20





**FIG. 22**

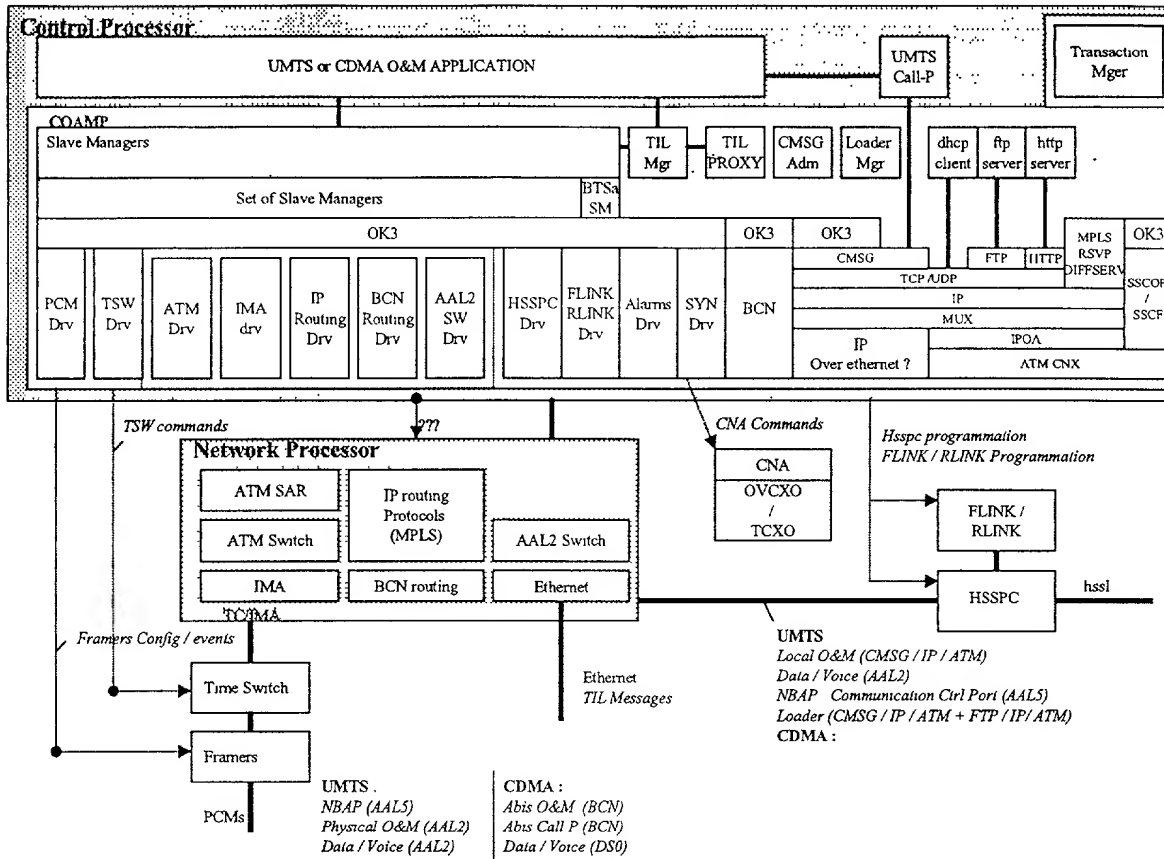


FIG. 23

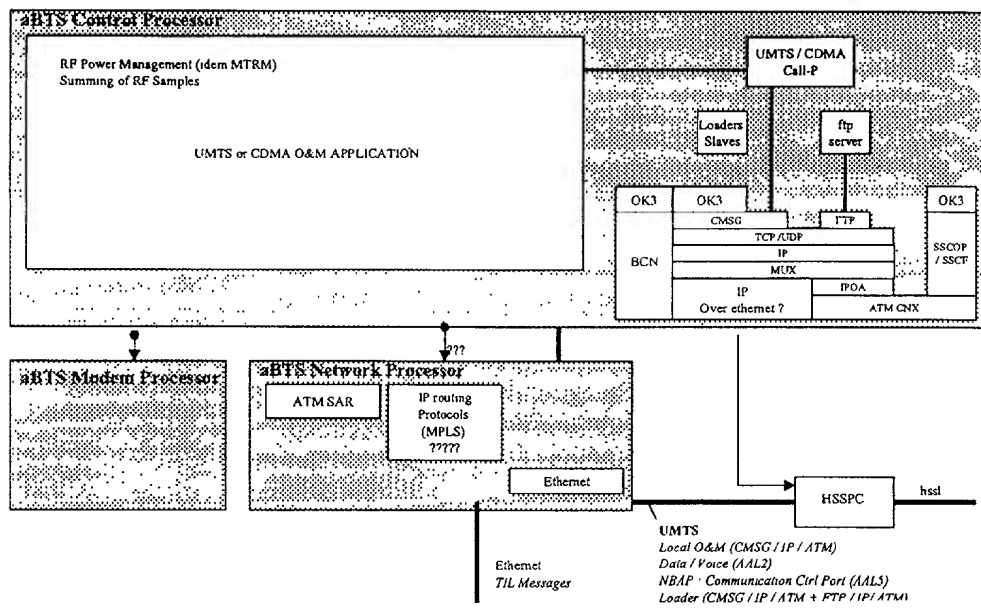


FIG. 24



2500

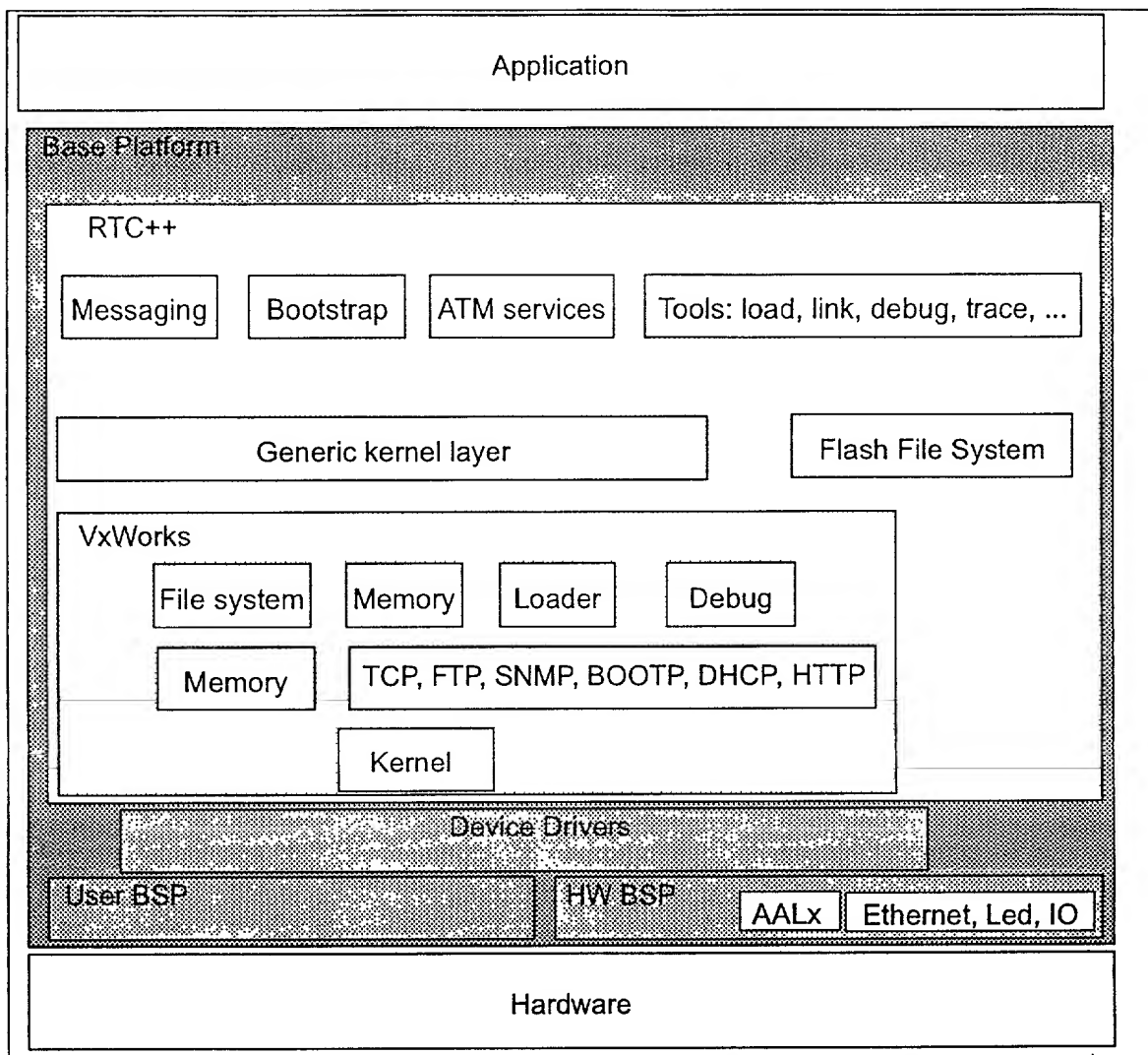


FIG. 25

2600

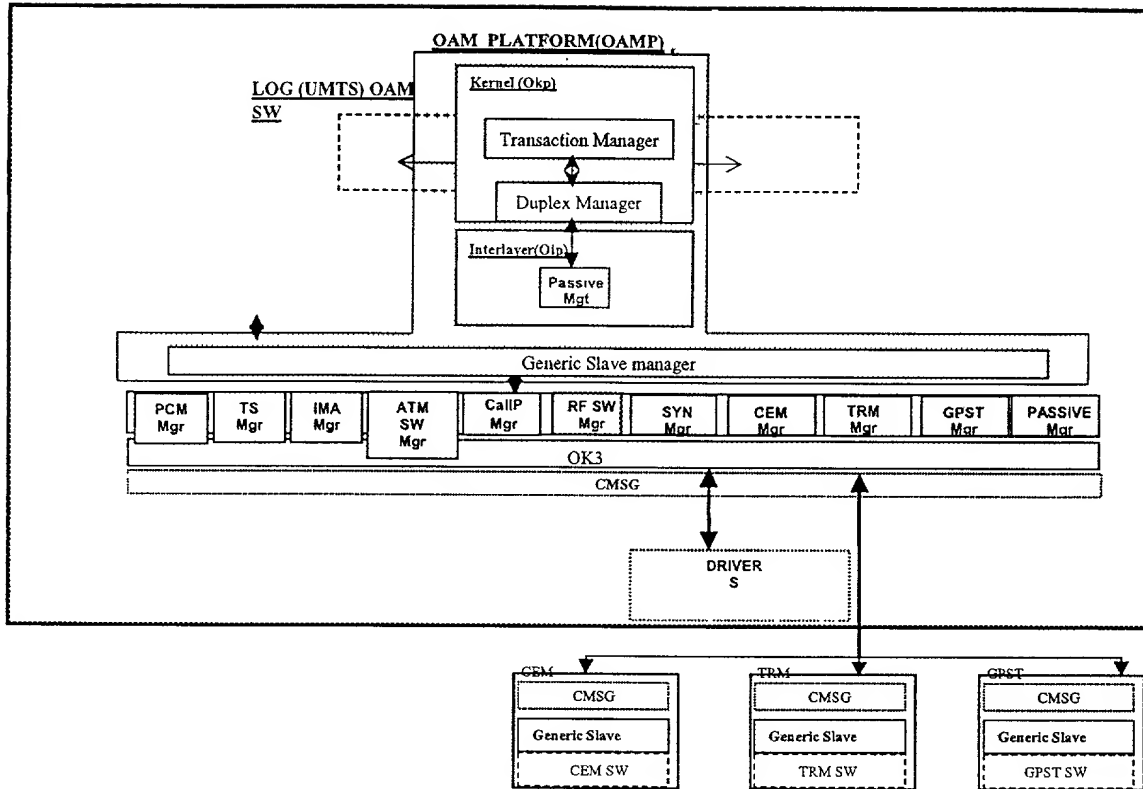


FIG. 26

2700

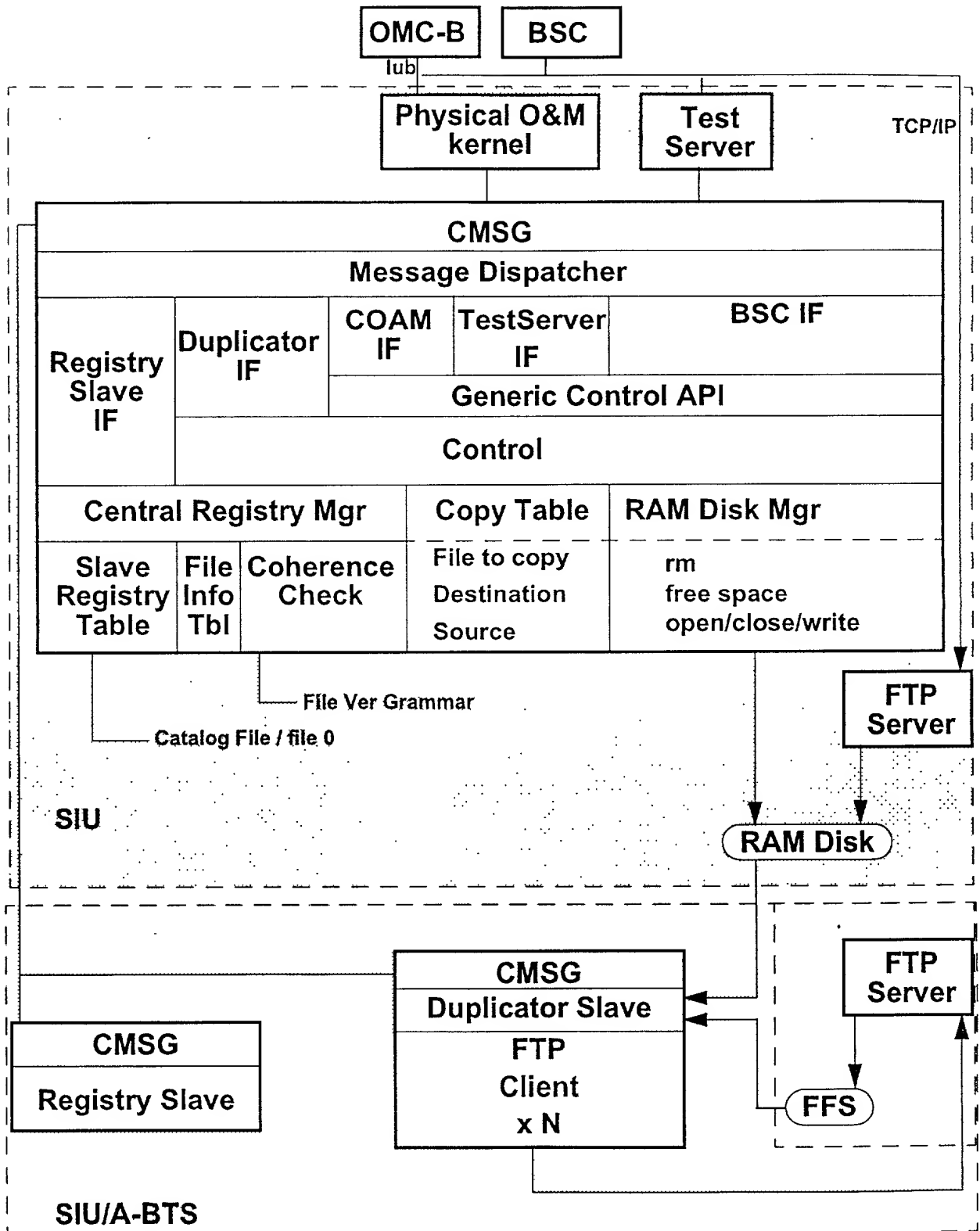


FIG. 27

2800

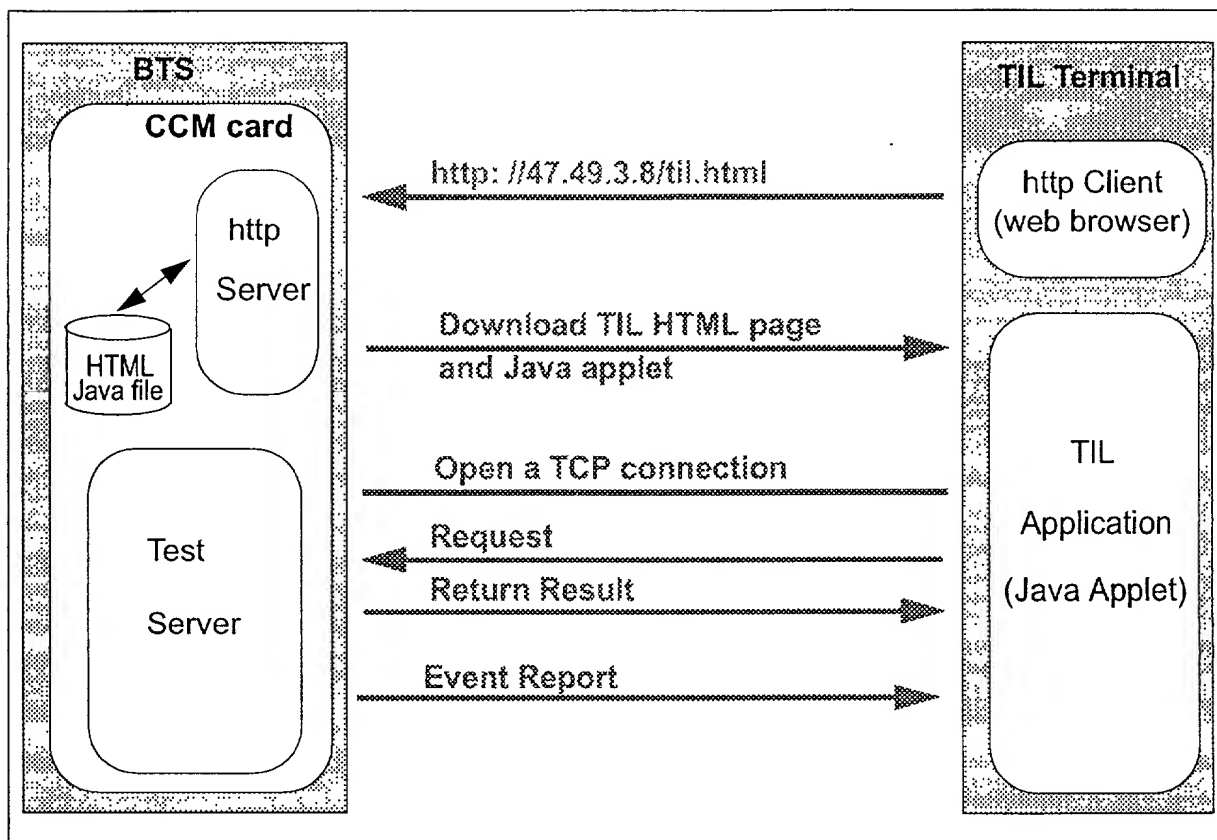
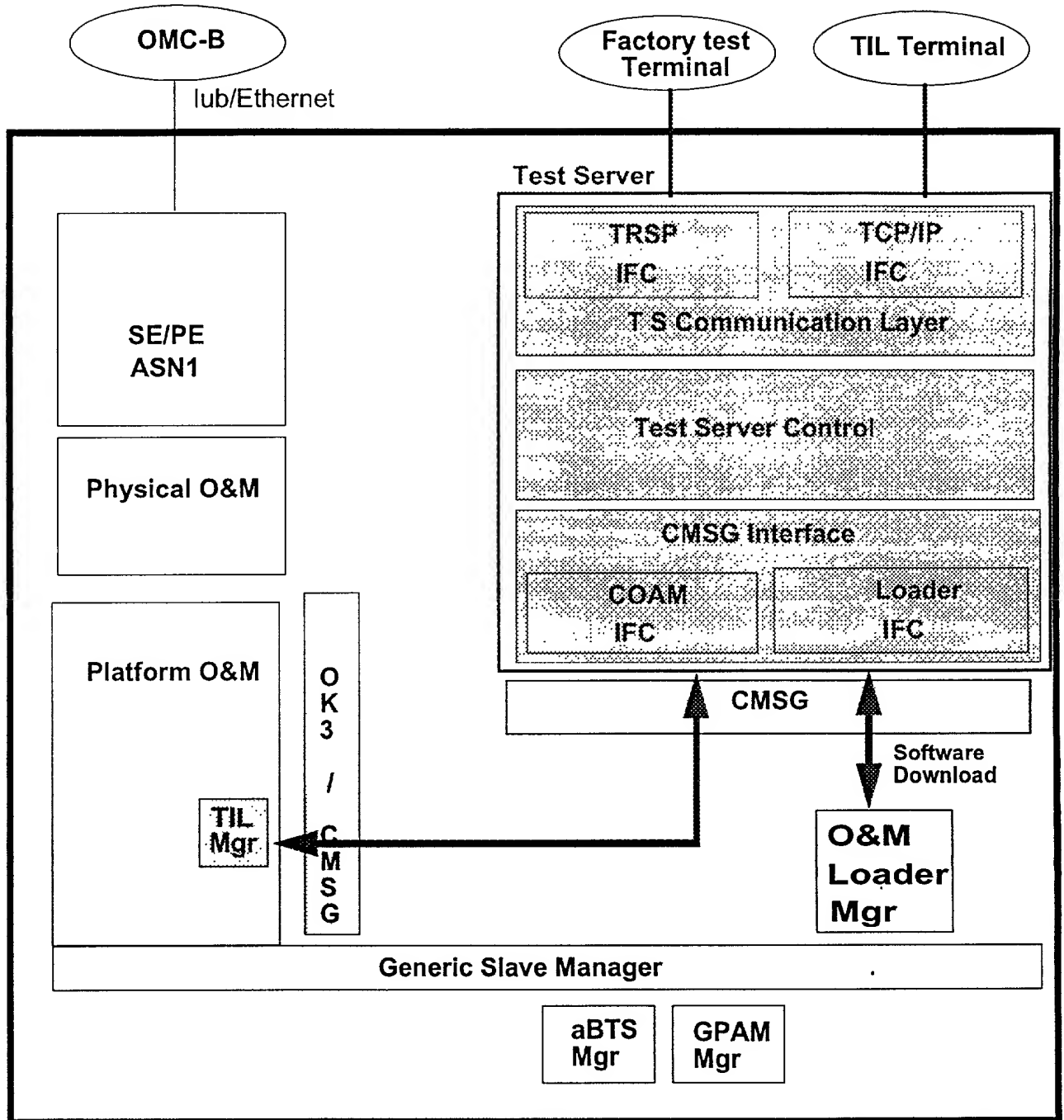


FIG. 28




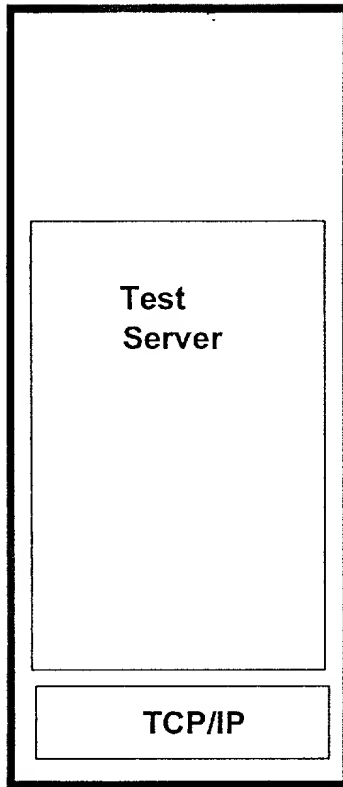
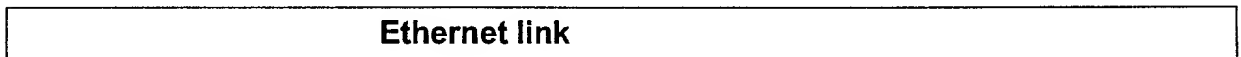
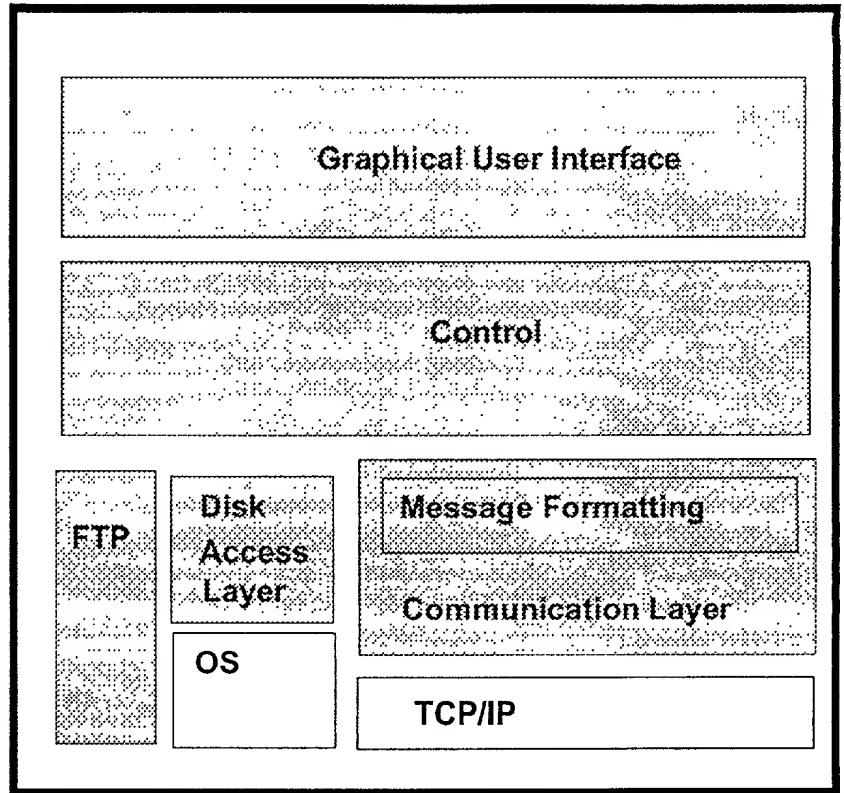
 Test Server layers

FIG. 29

SIU card



TIL Terminal



TIL Application Layers

FIG. 30

[illegible]

FIG. 31





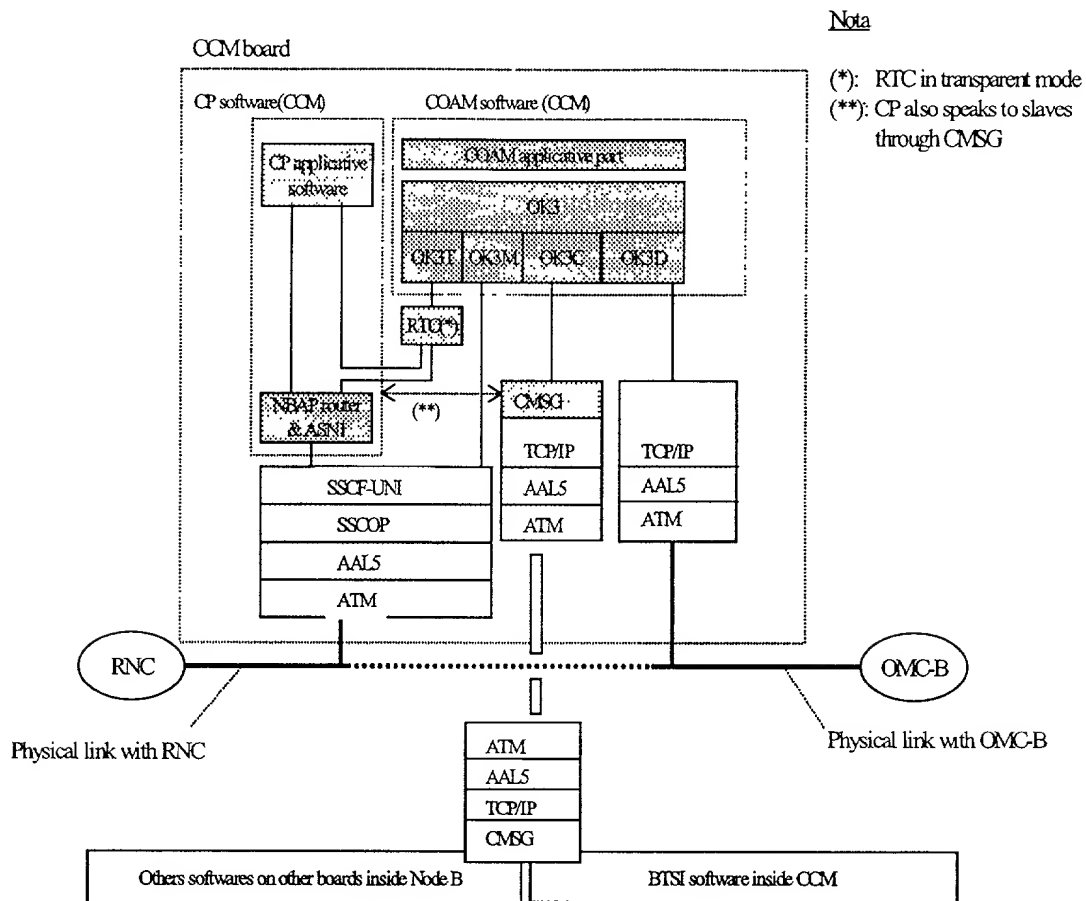


FIG. 33

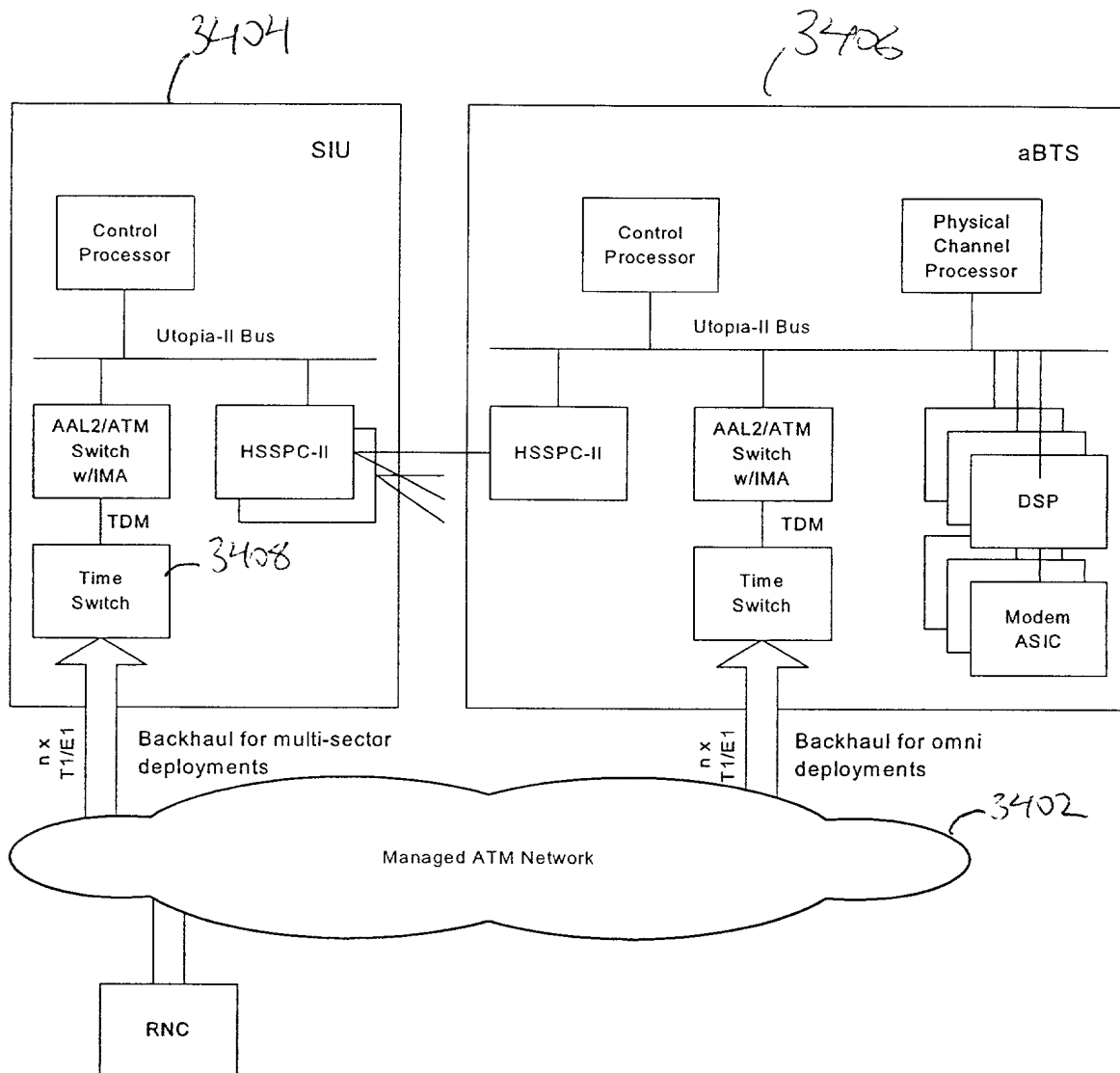


FIG. 34

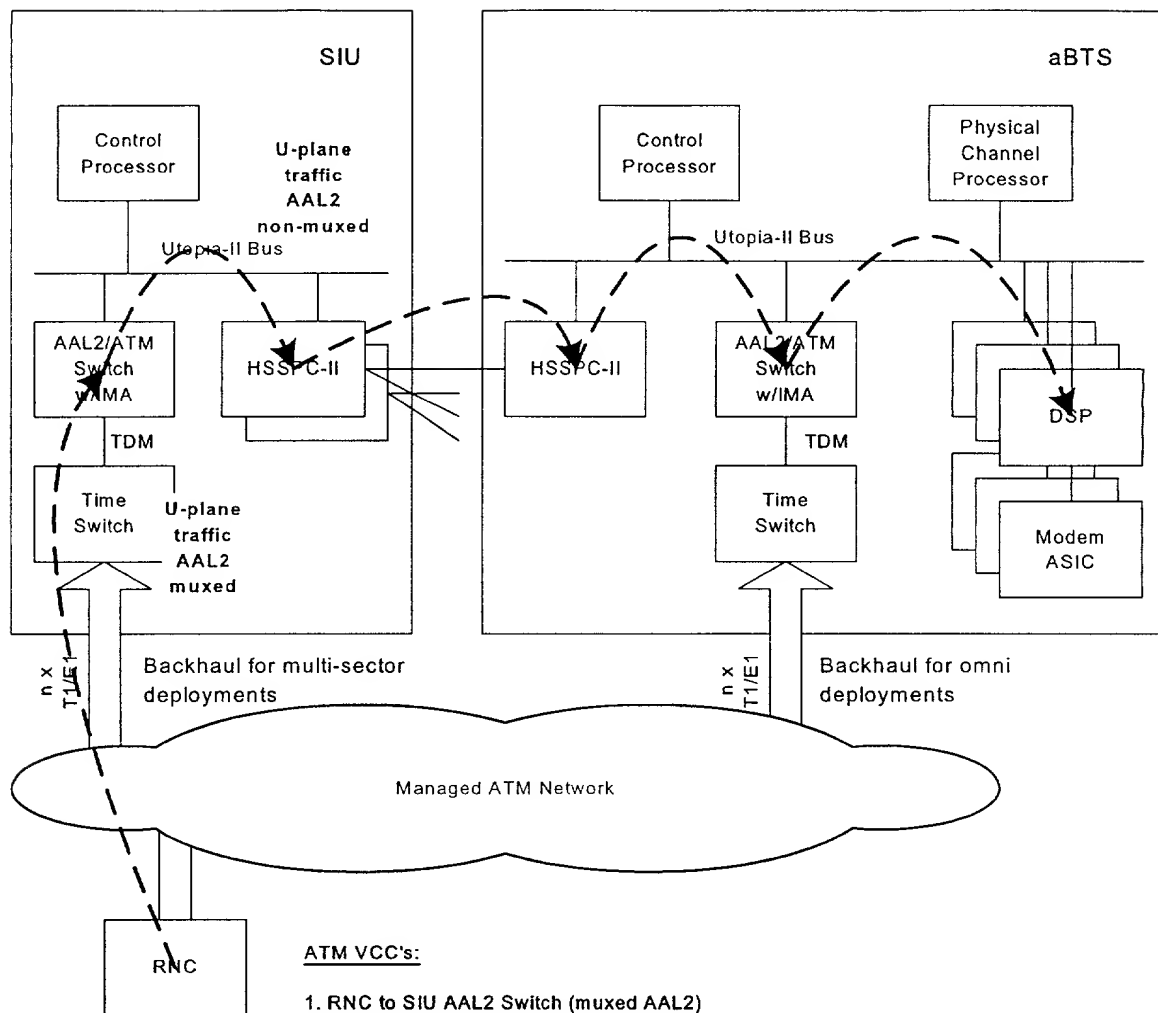


FIG. 35

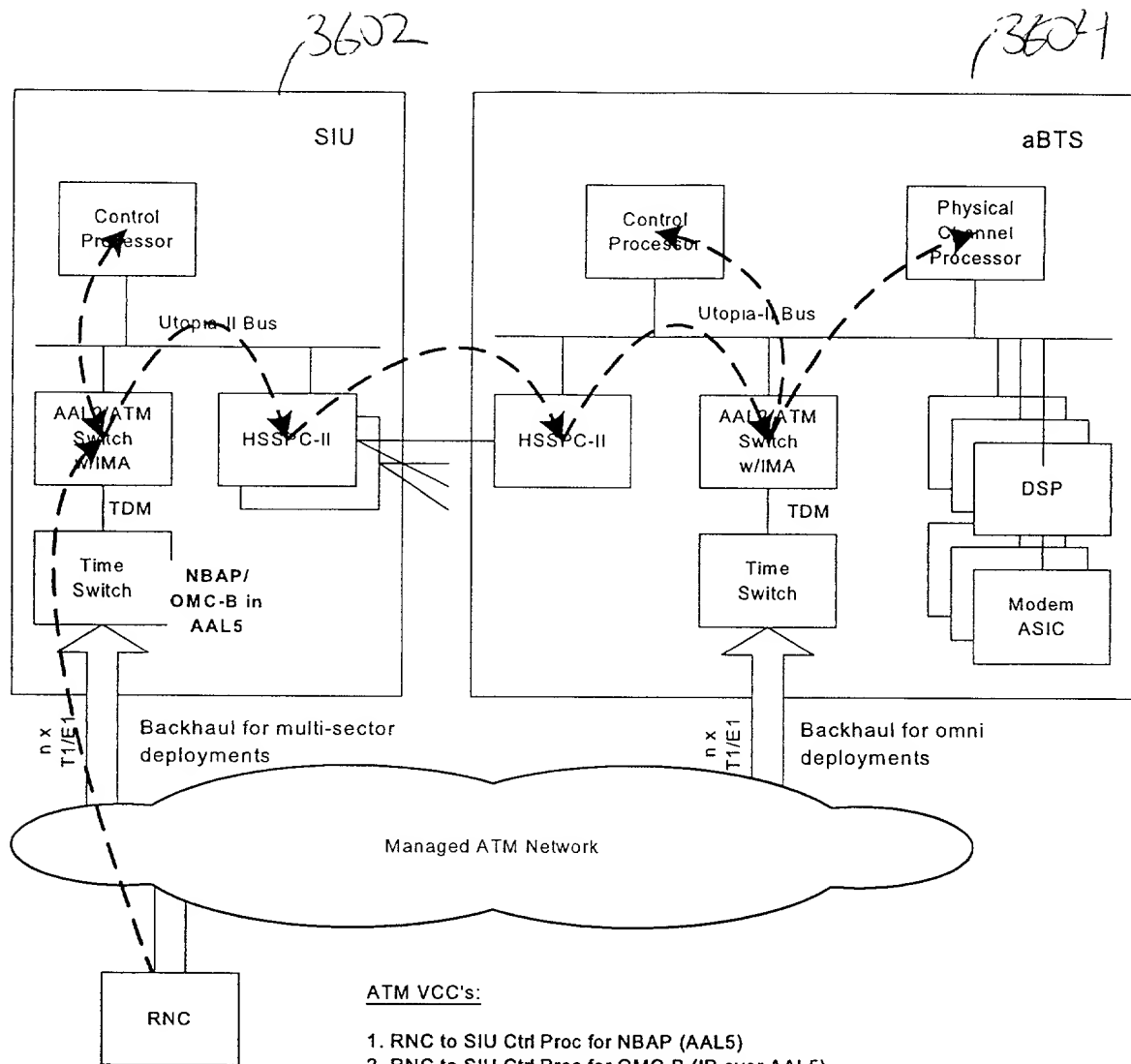


FIG. 36

1. The first step is to identify the components of the system.
 2. The second step is to determine the flow of data between these components.
 3. The third step is to create a diagram that represents this flow.
 4. The fourth step is to label the components and the flow lines.
 5. The fifth step is to review the diagram for accuracy.

# UITS '99 (ATM backhaul) NBAP Flow

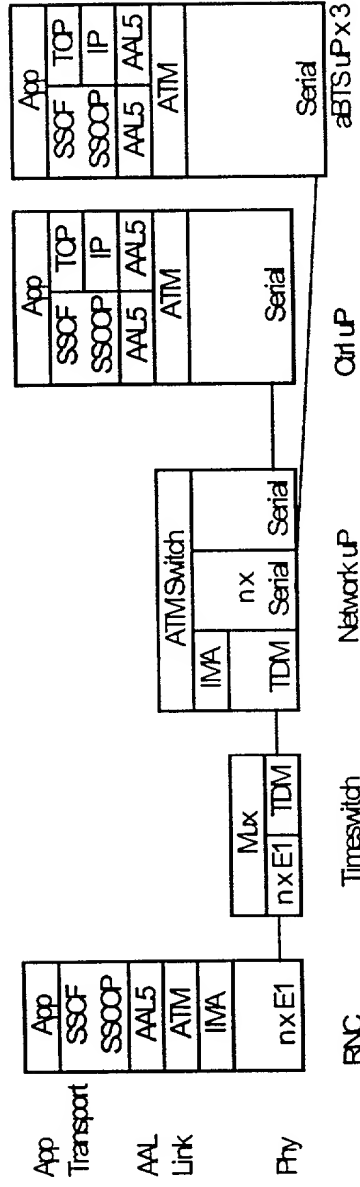


FIG. 37

UMTS '99 (ATM backhaul) QMC-B Flow

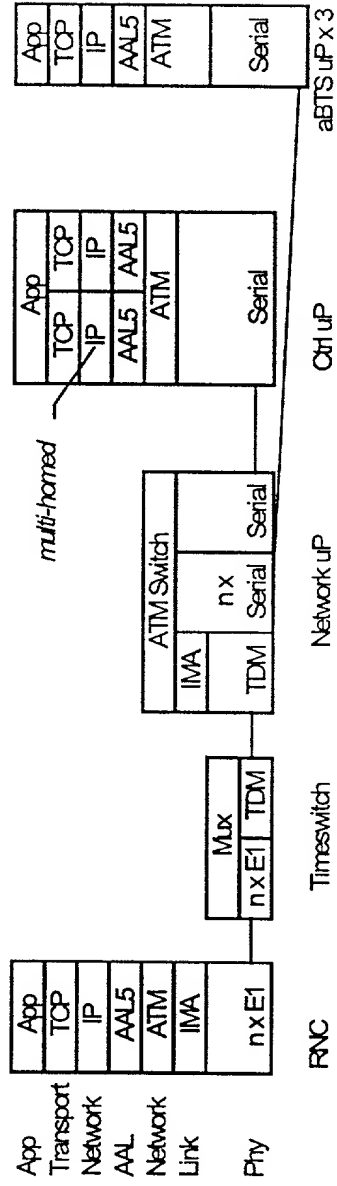


FIG. 38

UMTS '99 (ATM backhaul) User Flow

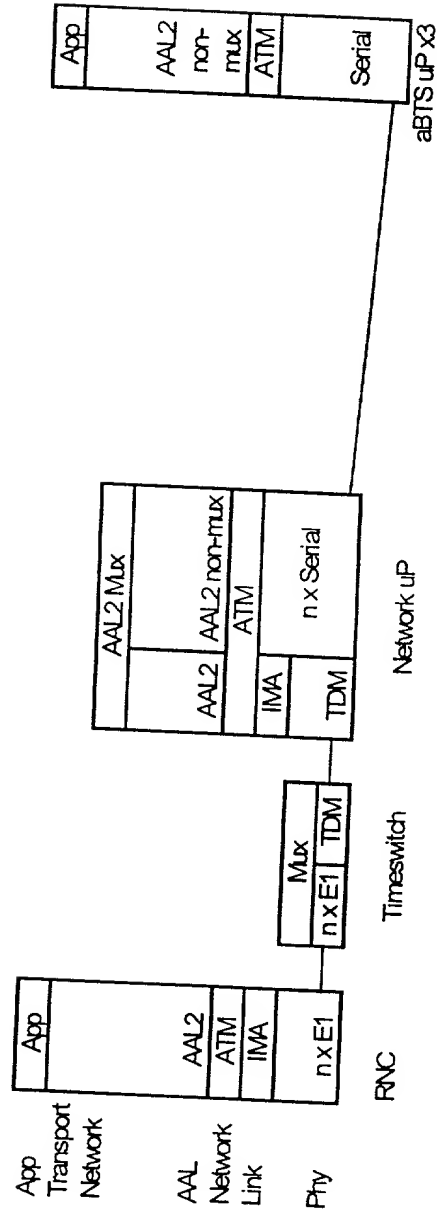
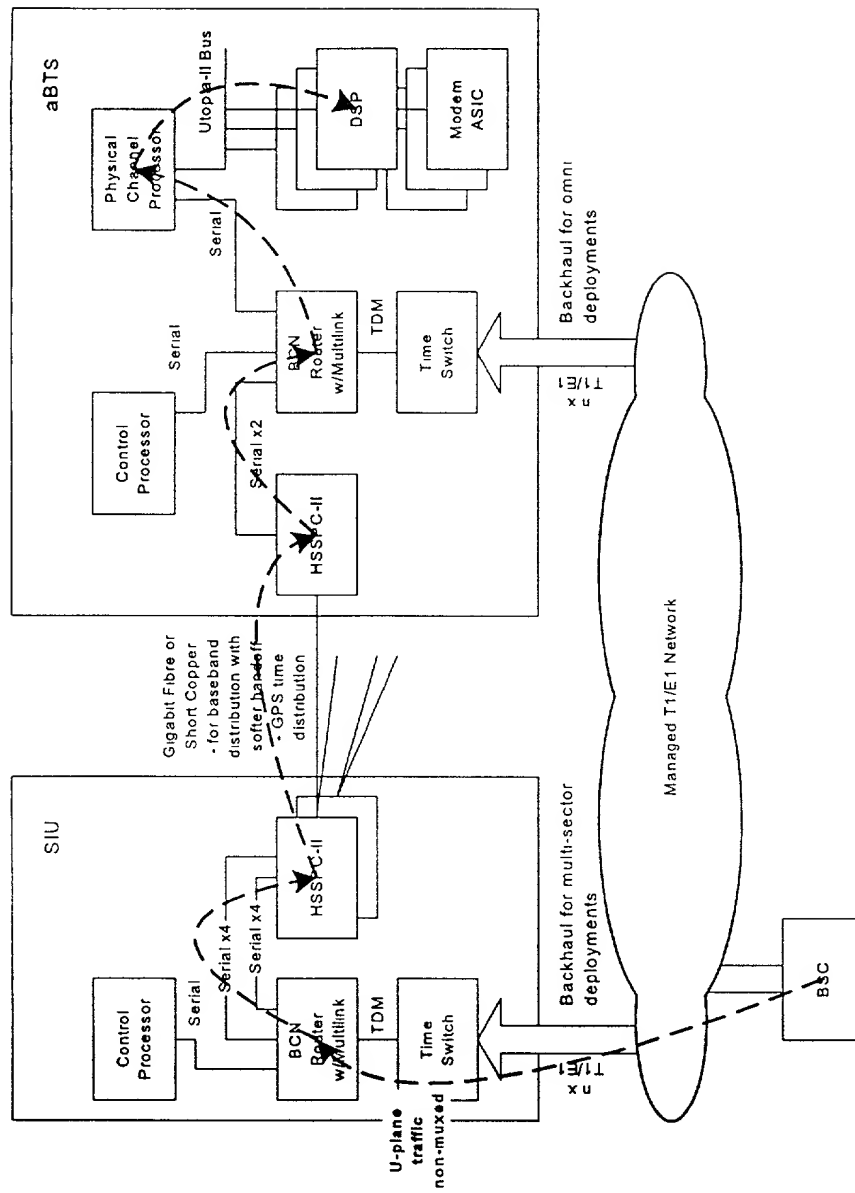


FIG. 39







FILE 17

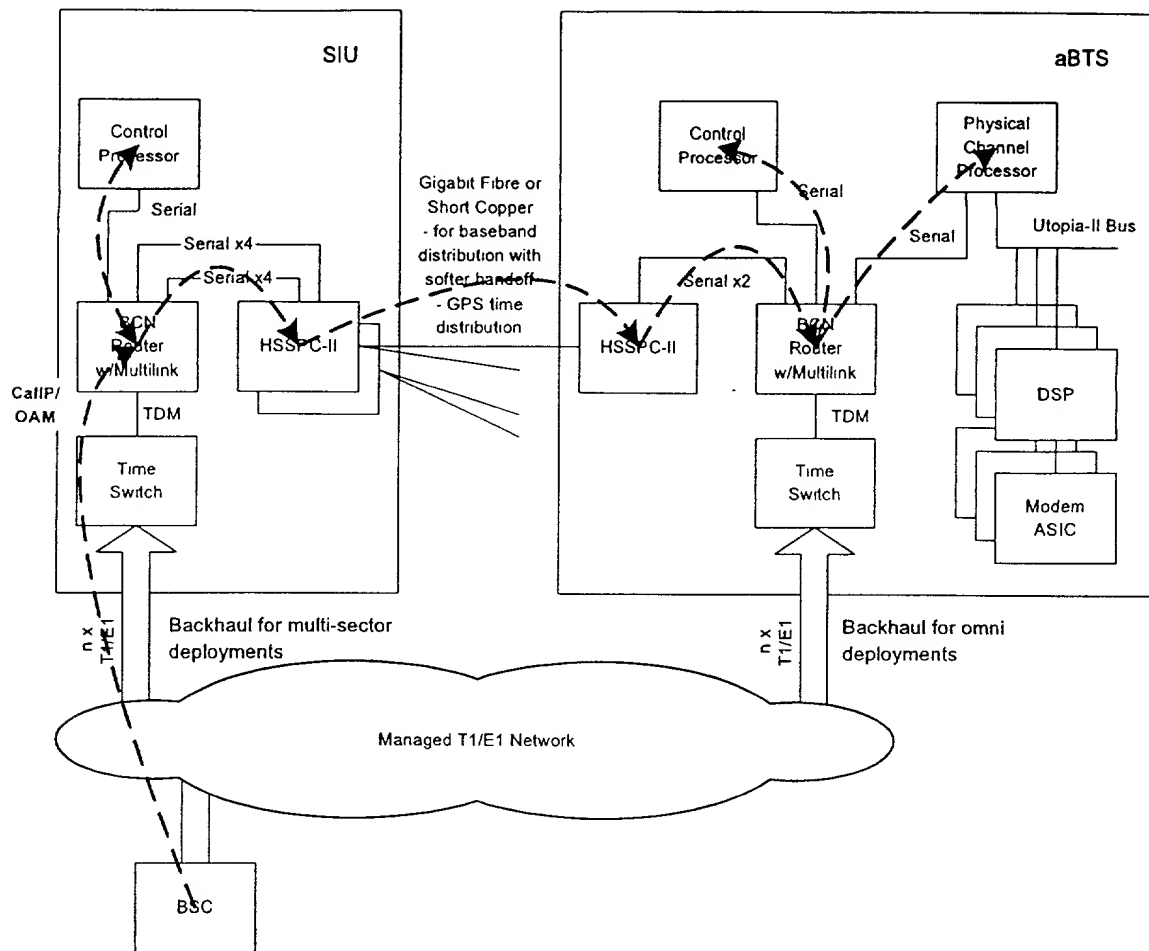


FIG. 42

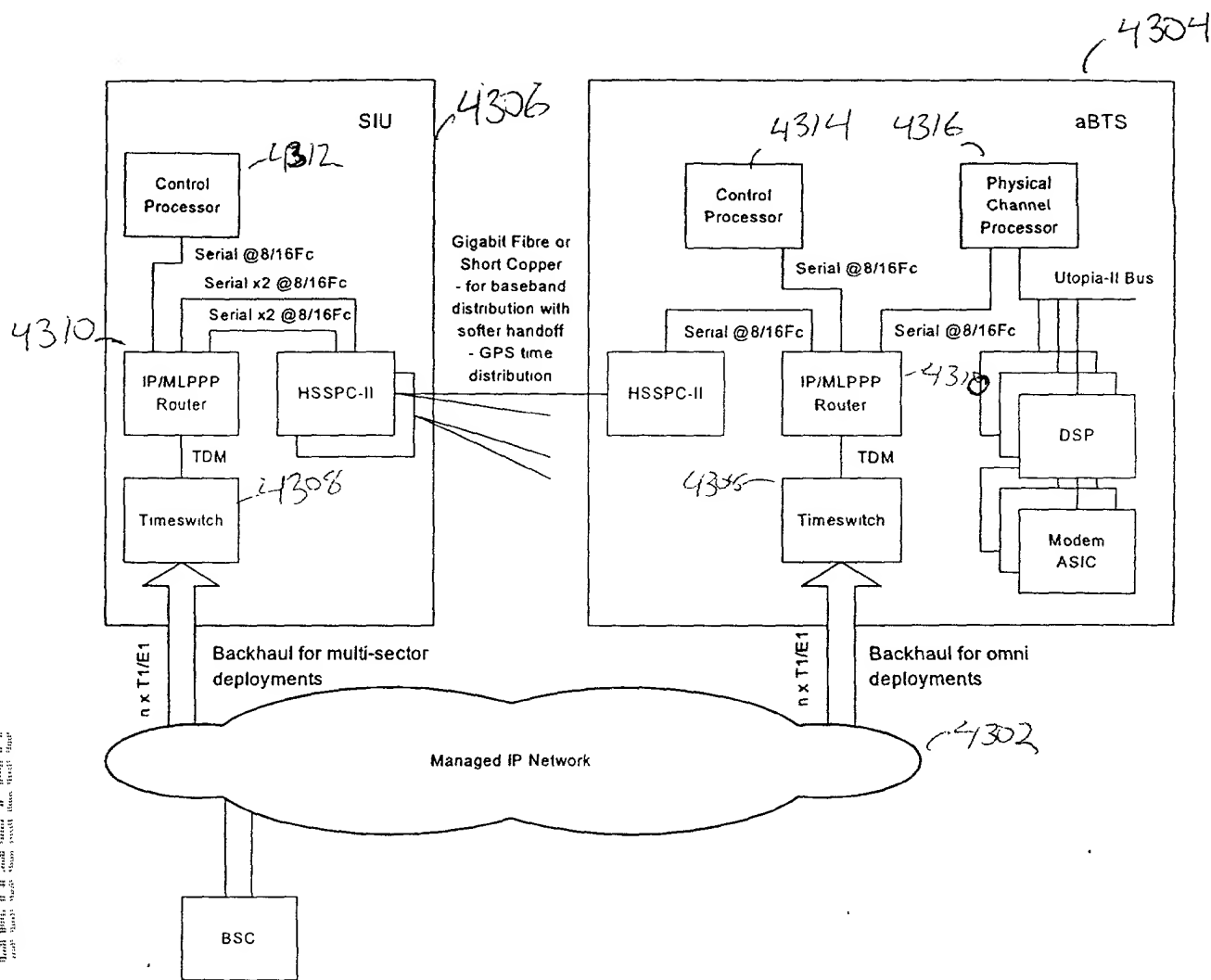


FIG. 43

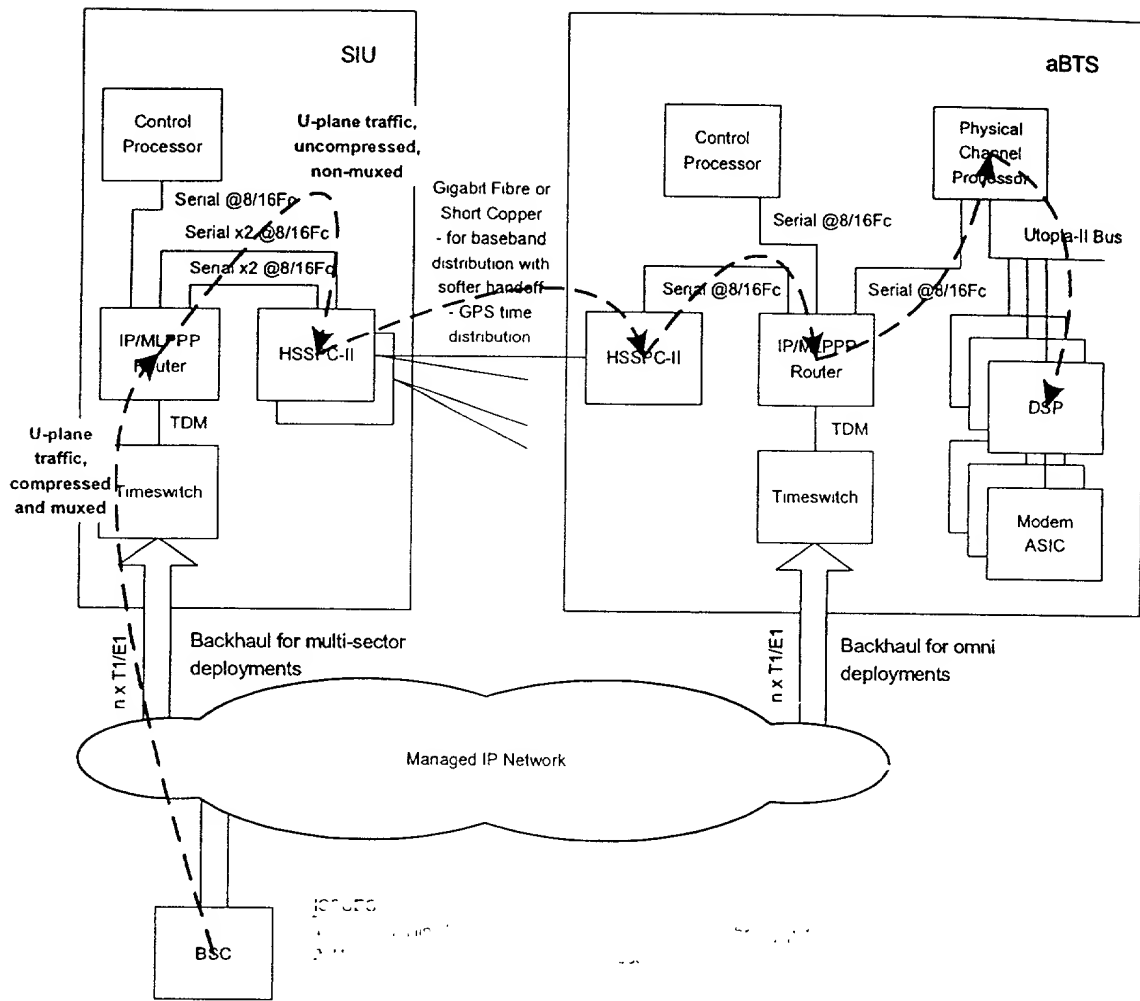


FIG. 44

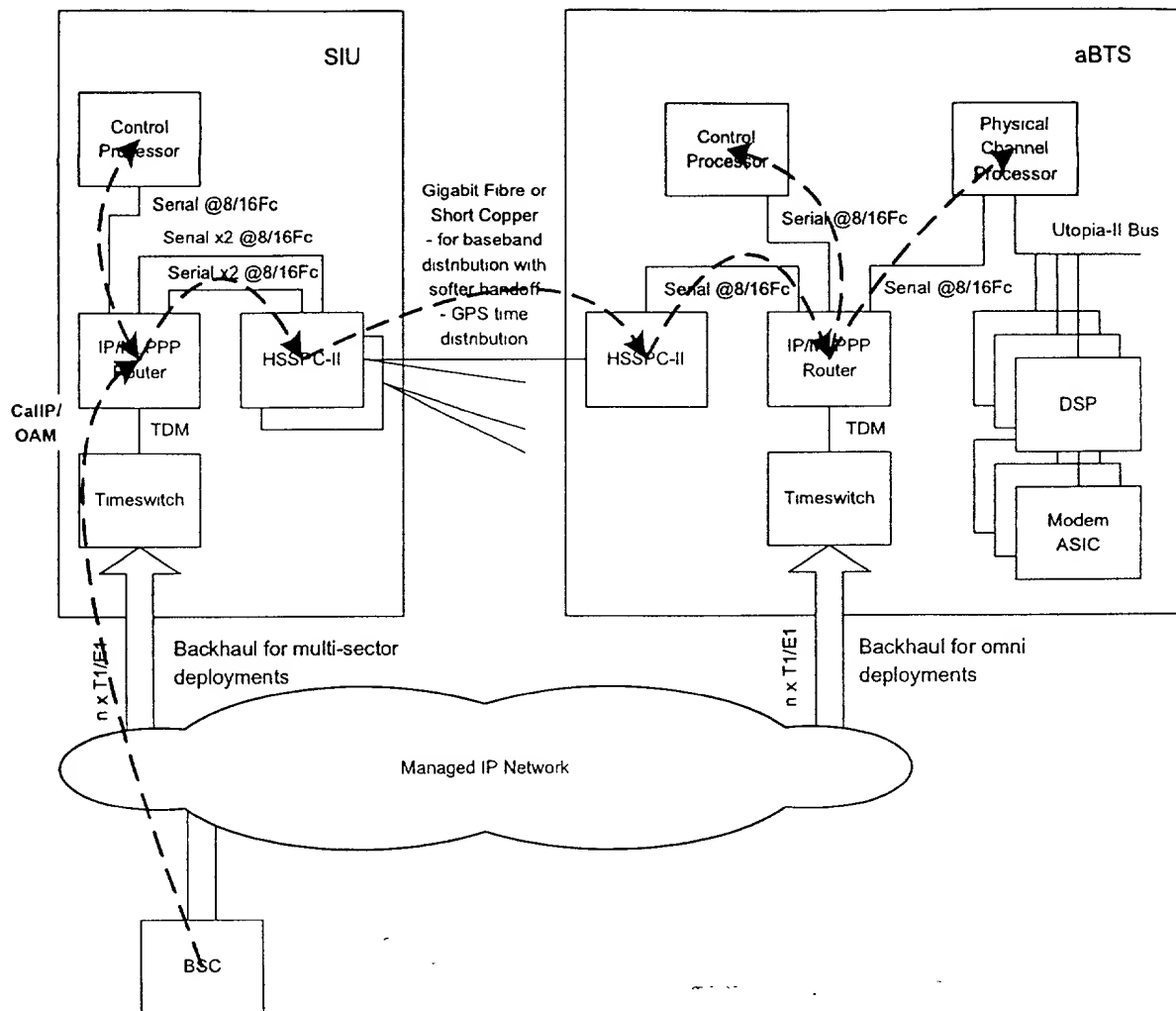


FIG. 45

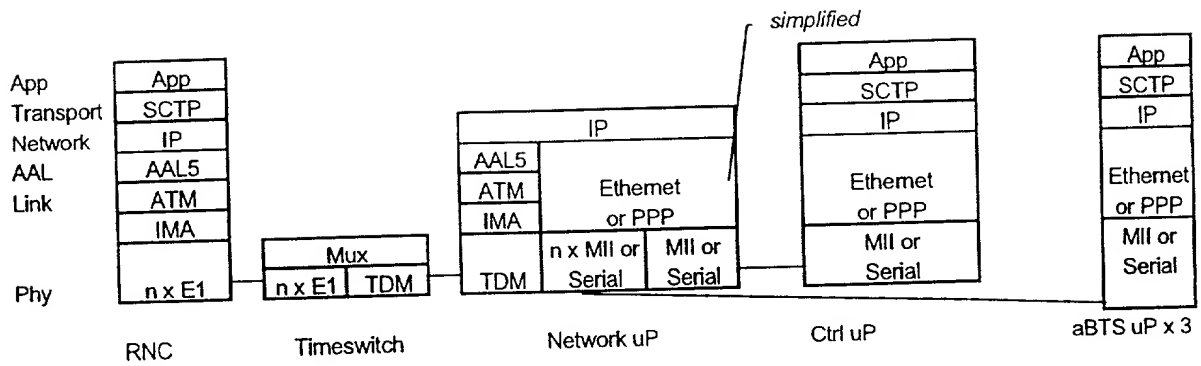


FIG. 46

UMTS '00 (IPoA backhaul) OMC-B Flow / CDMA OAM

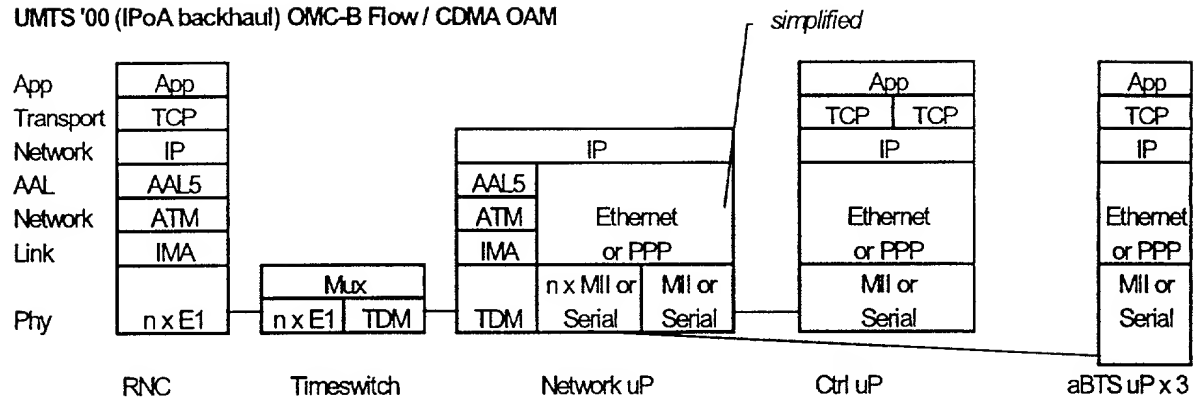


FIG. 47

UMTS '00 (IPoA backhaul) User Flow / CDMA A.bis User Traffic

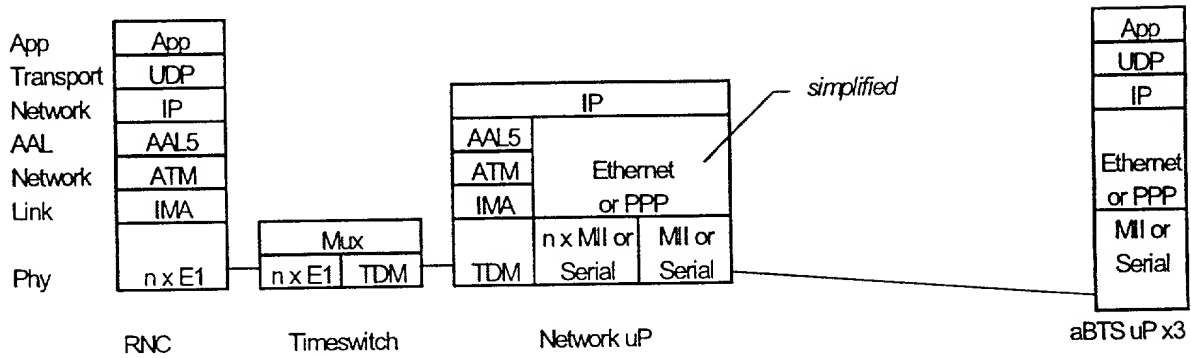


FIG. 48



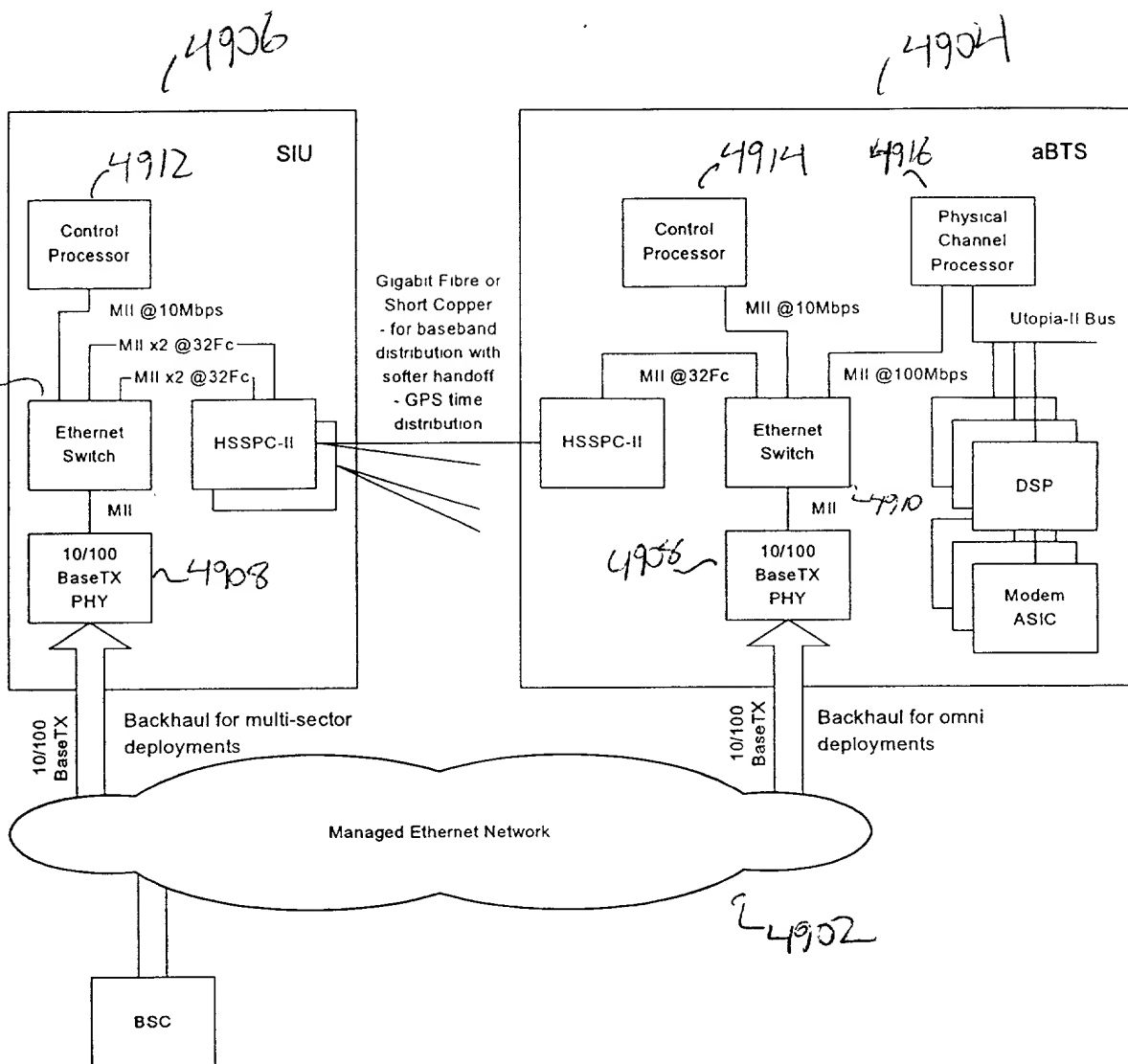


FIG. 49

UMTS '00 (IP/Ethernet backhaul) NBAP Flow / CDMA A.bis

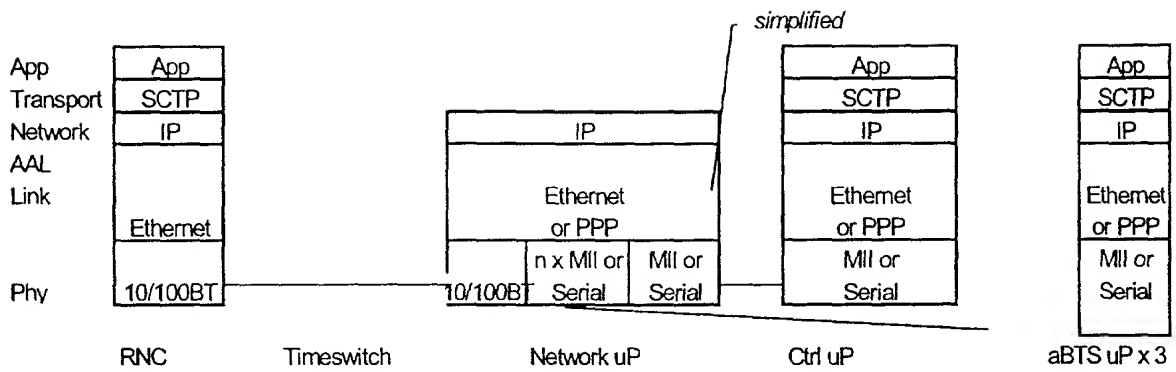


FIG. 50

UMTS '00 (IP/Ethernet backhaul) User Flow / CDMA A.bis

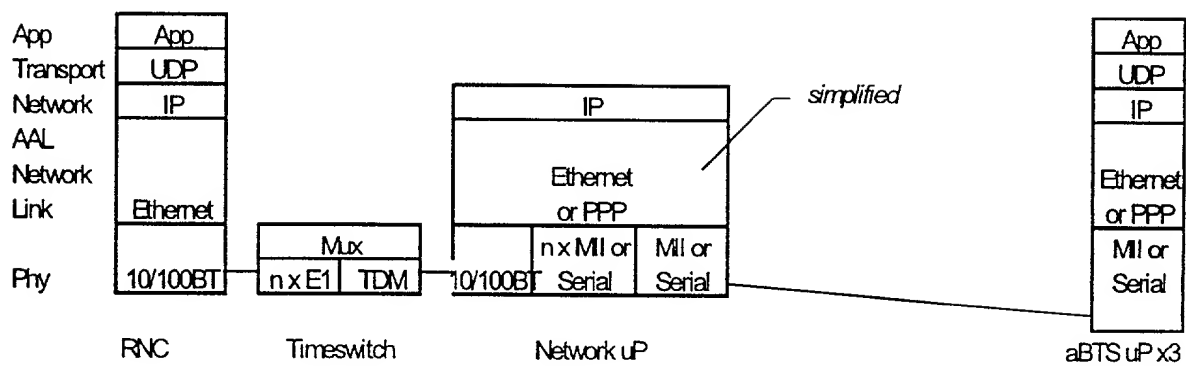


FIG. 51

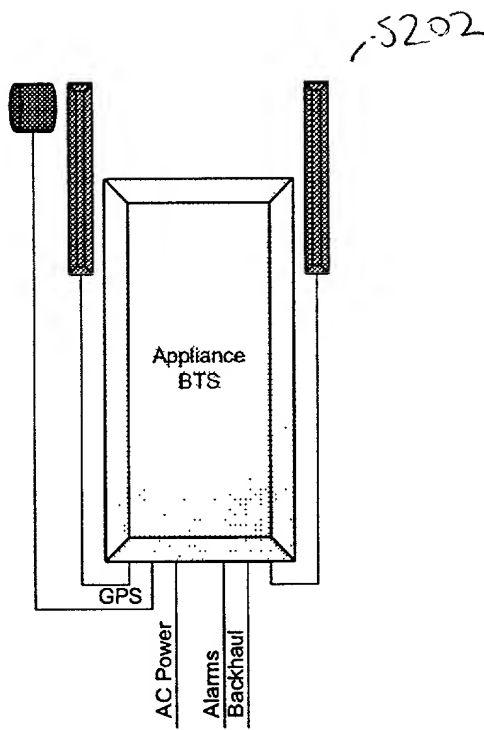


FIG. 52

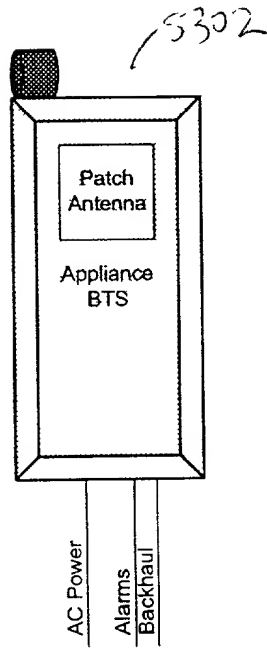


FIG. 53

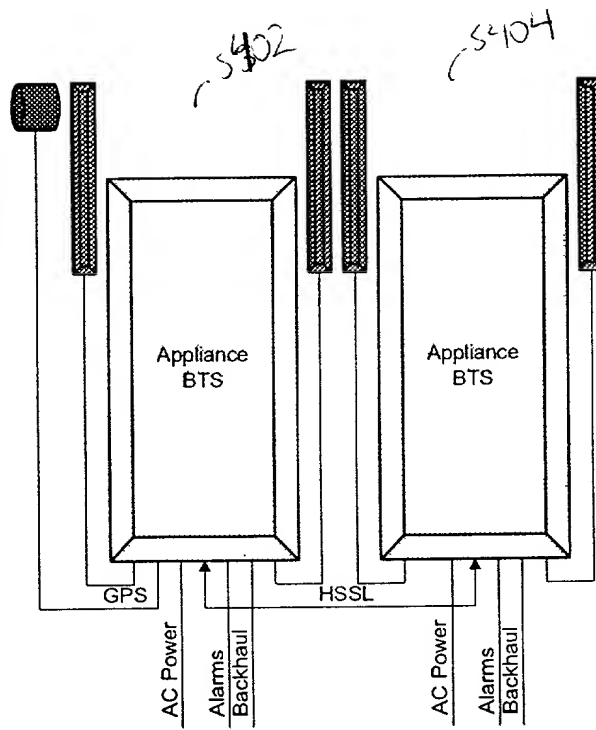


FIG. 54

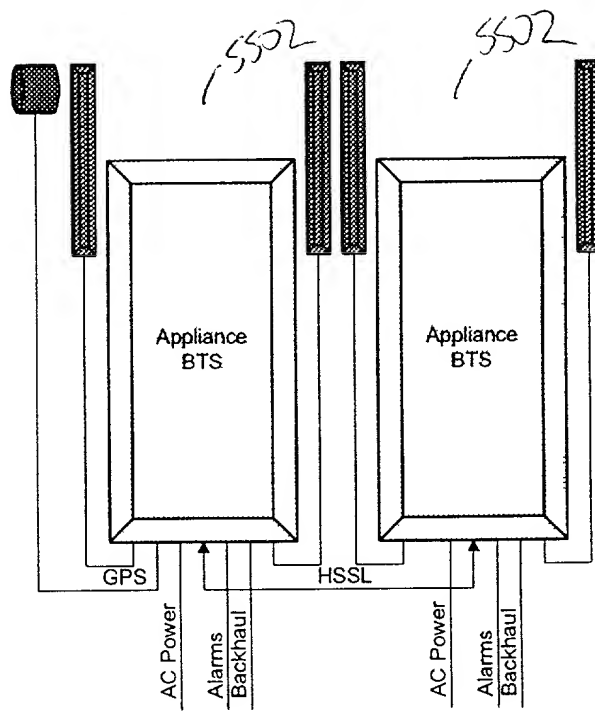


FIG. 55

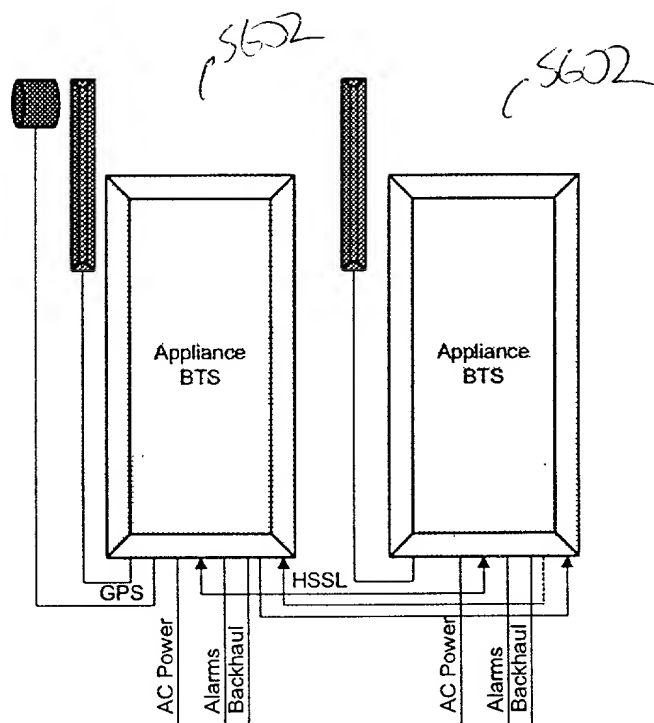


FIG. 56



5702

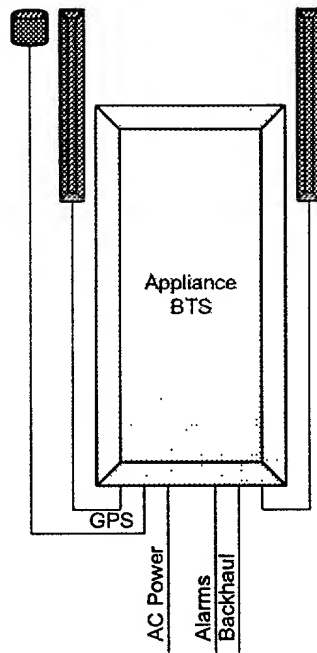


FIG. 57

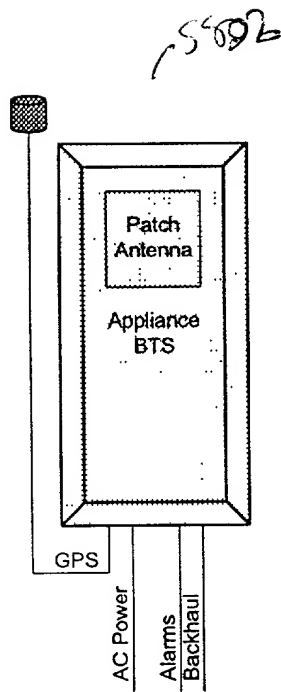


FIG. 58

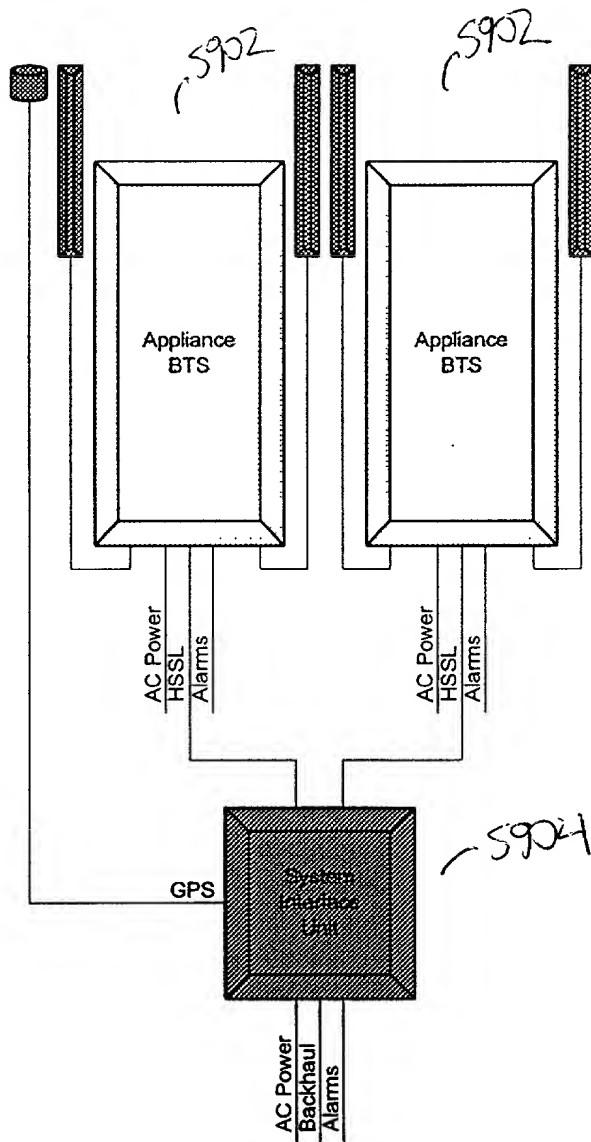


FIG. 59

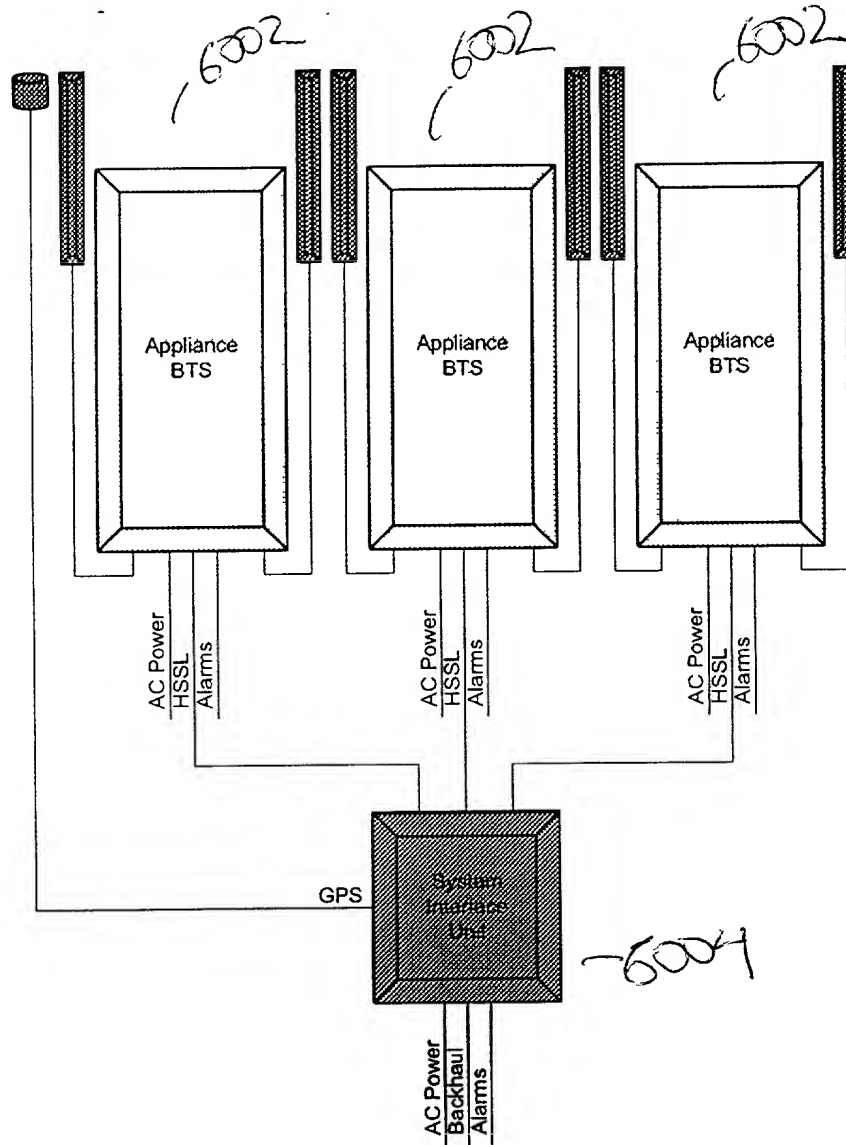


FIG. 60

6102

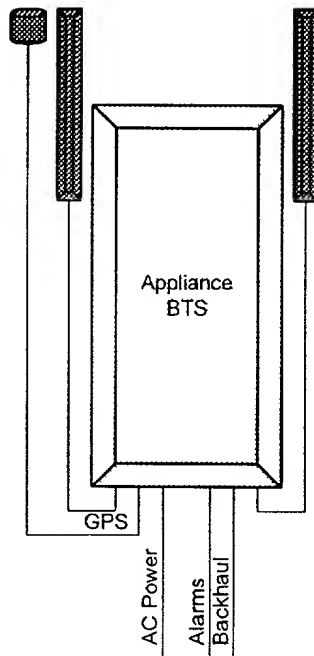


FIG. 61

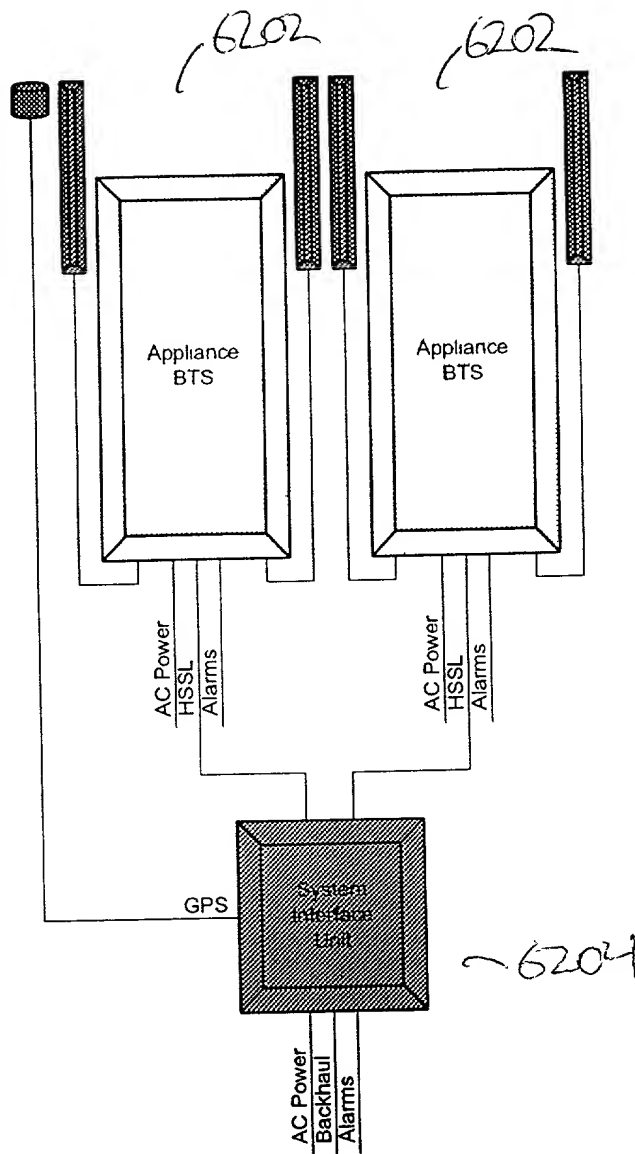


FIG. 62

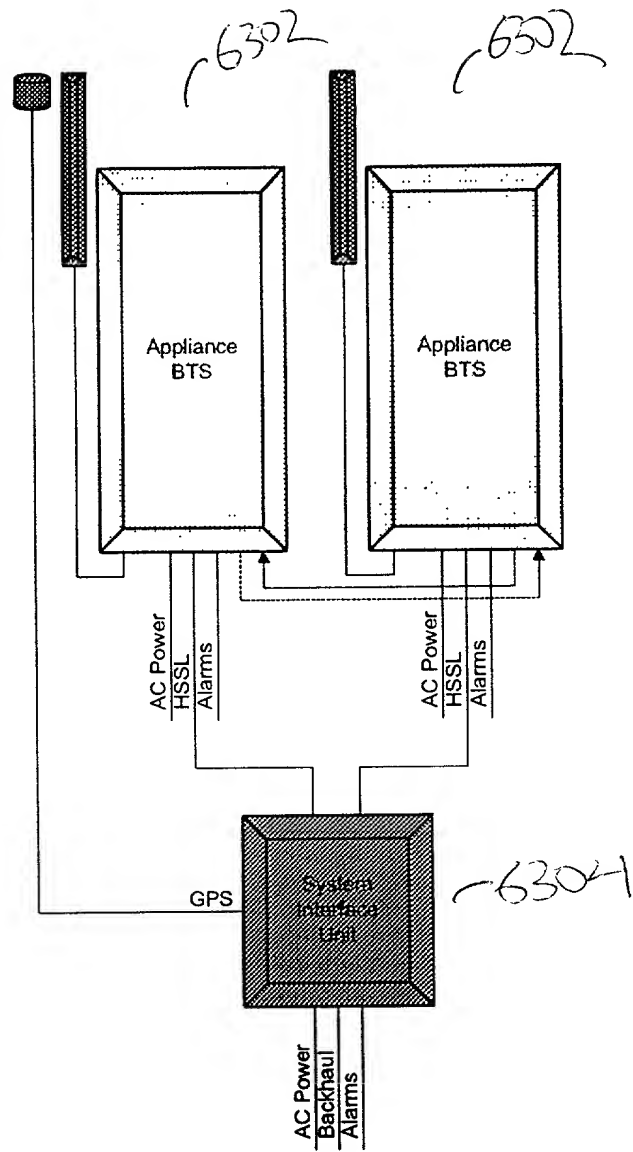


FIG. 63

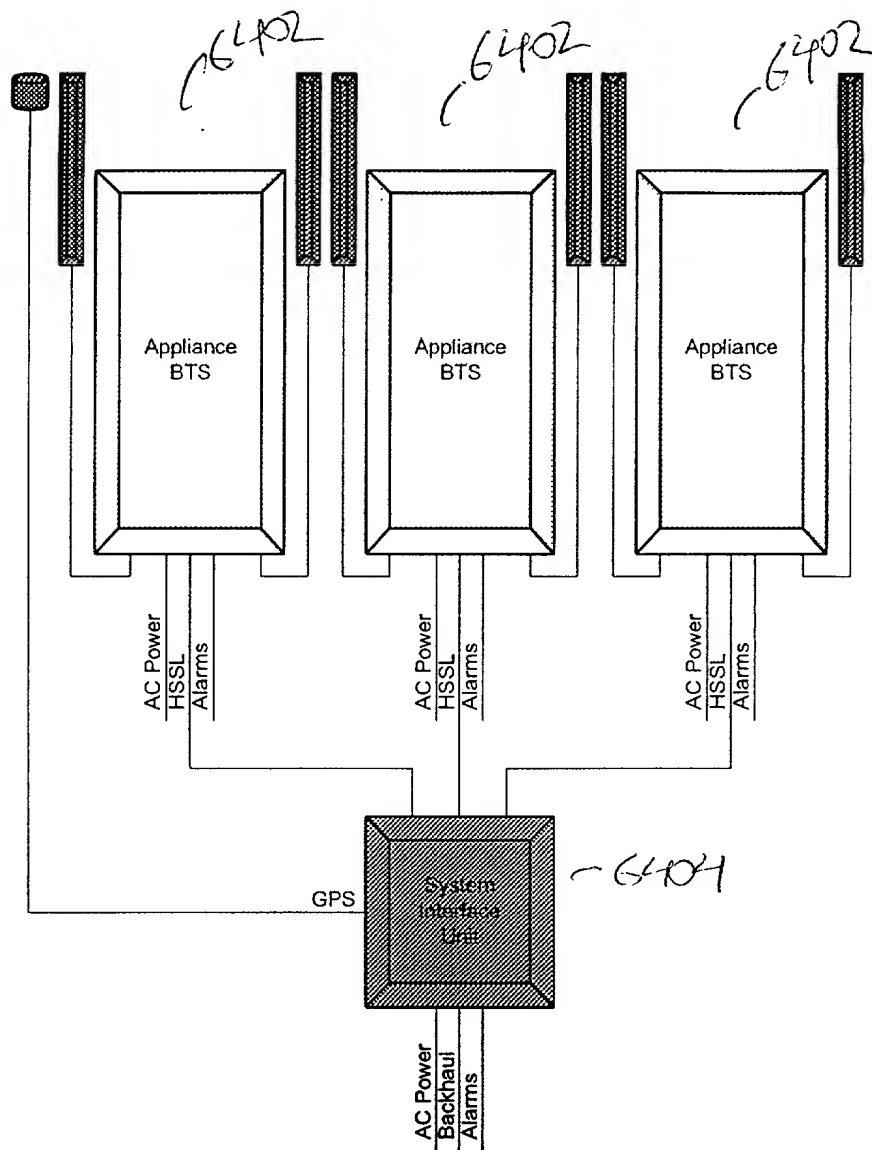


FIG. 64



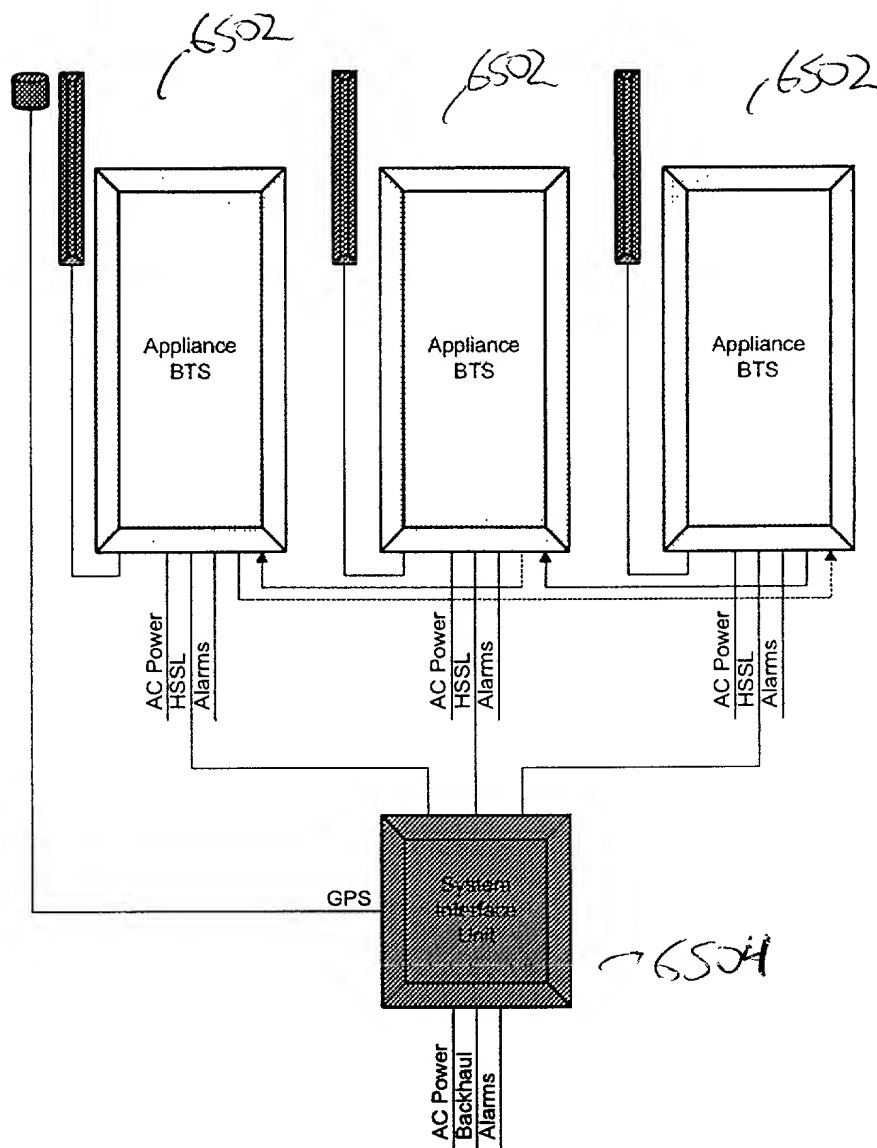


FIG. 65

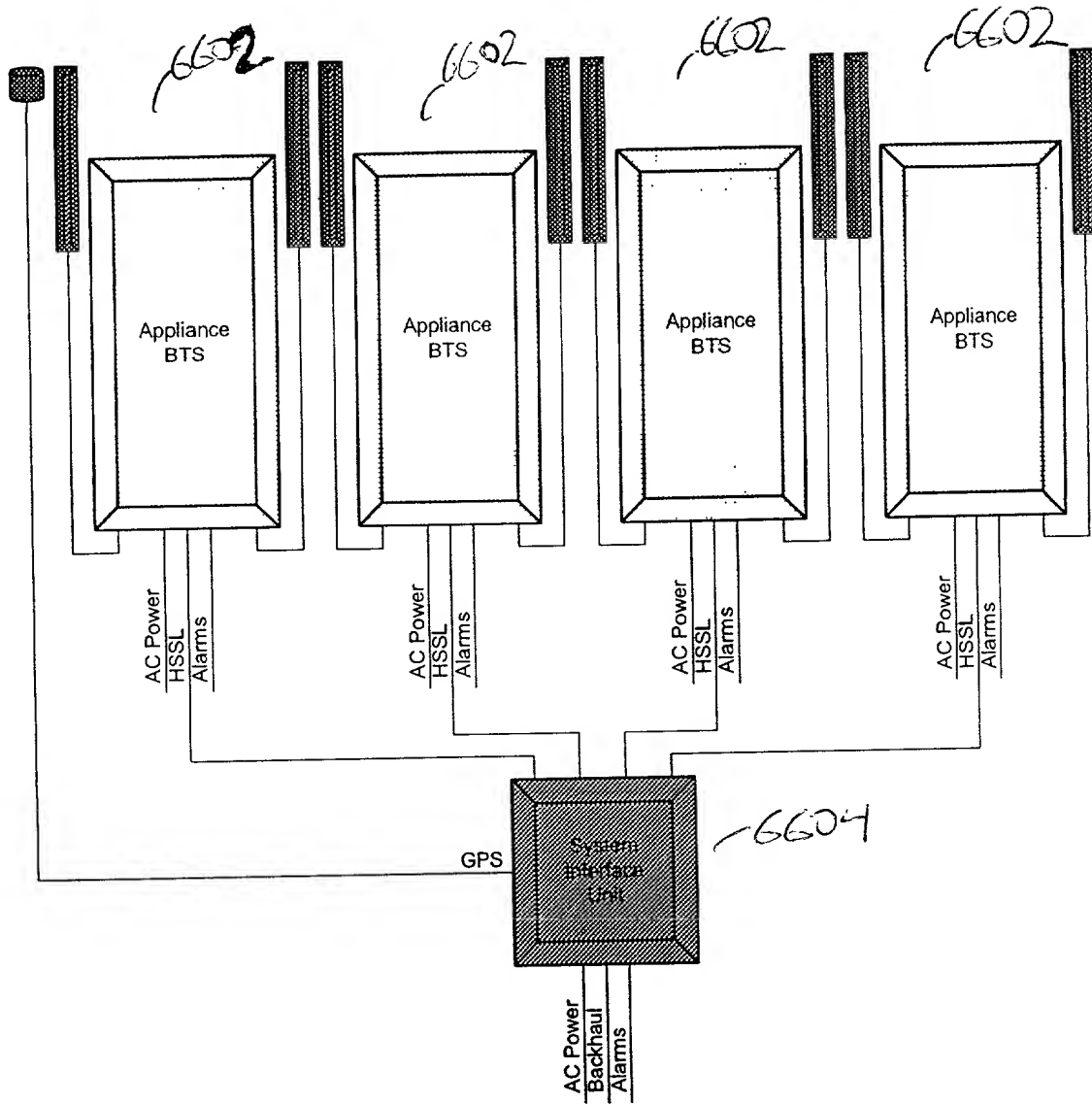


FIG.66

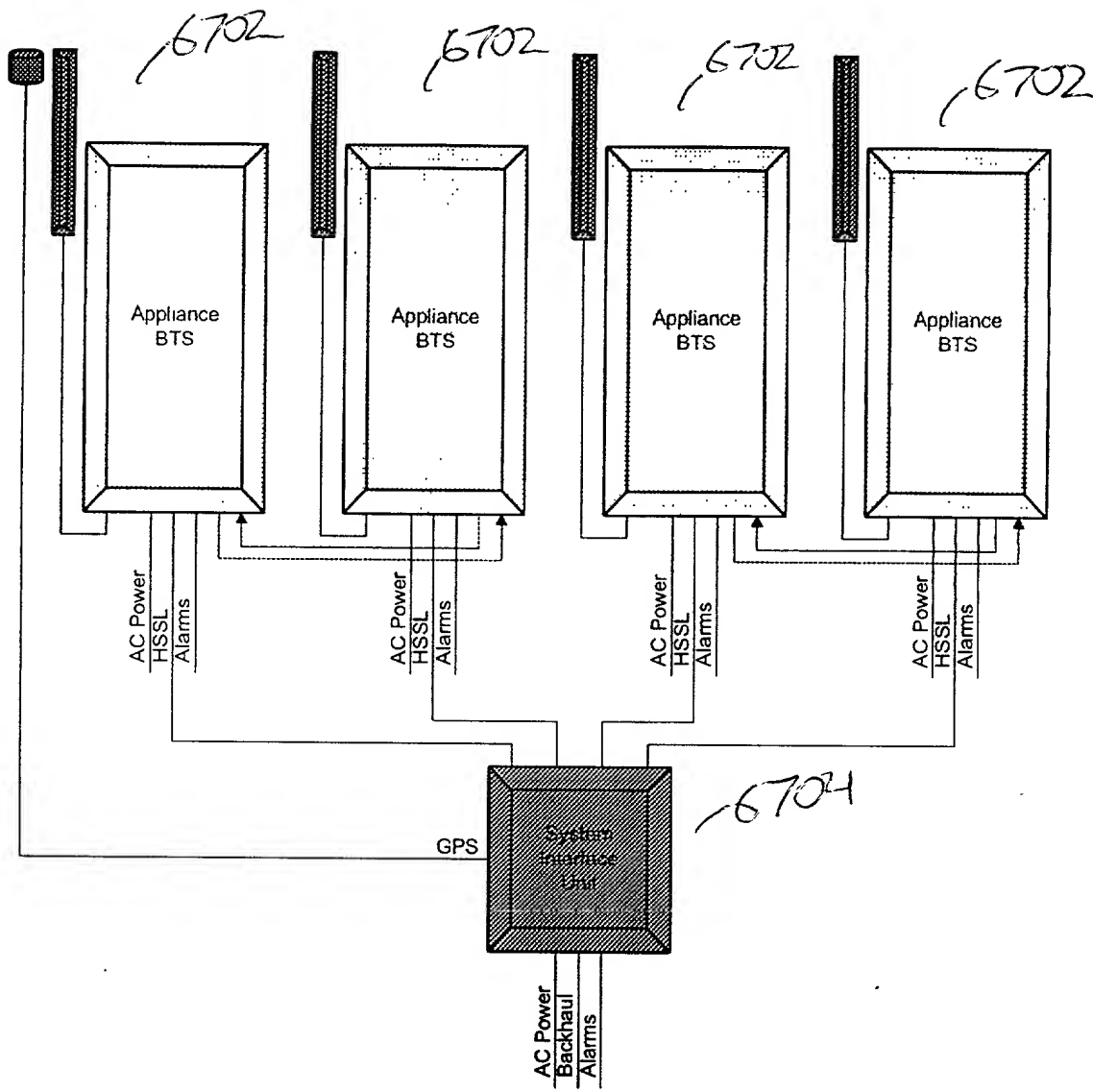


FIG. 67

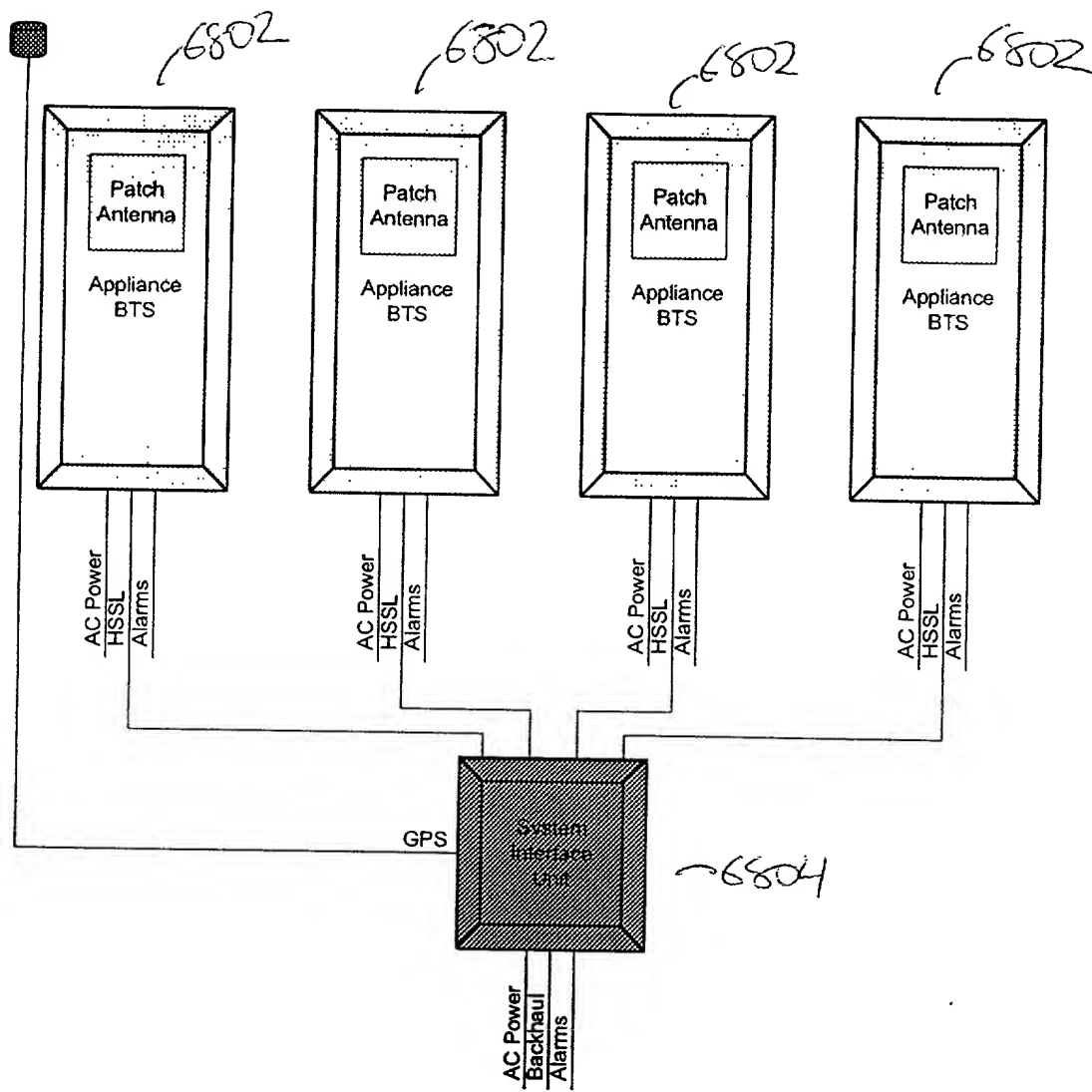


FIG. 68

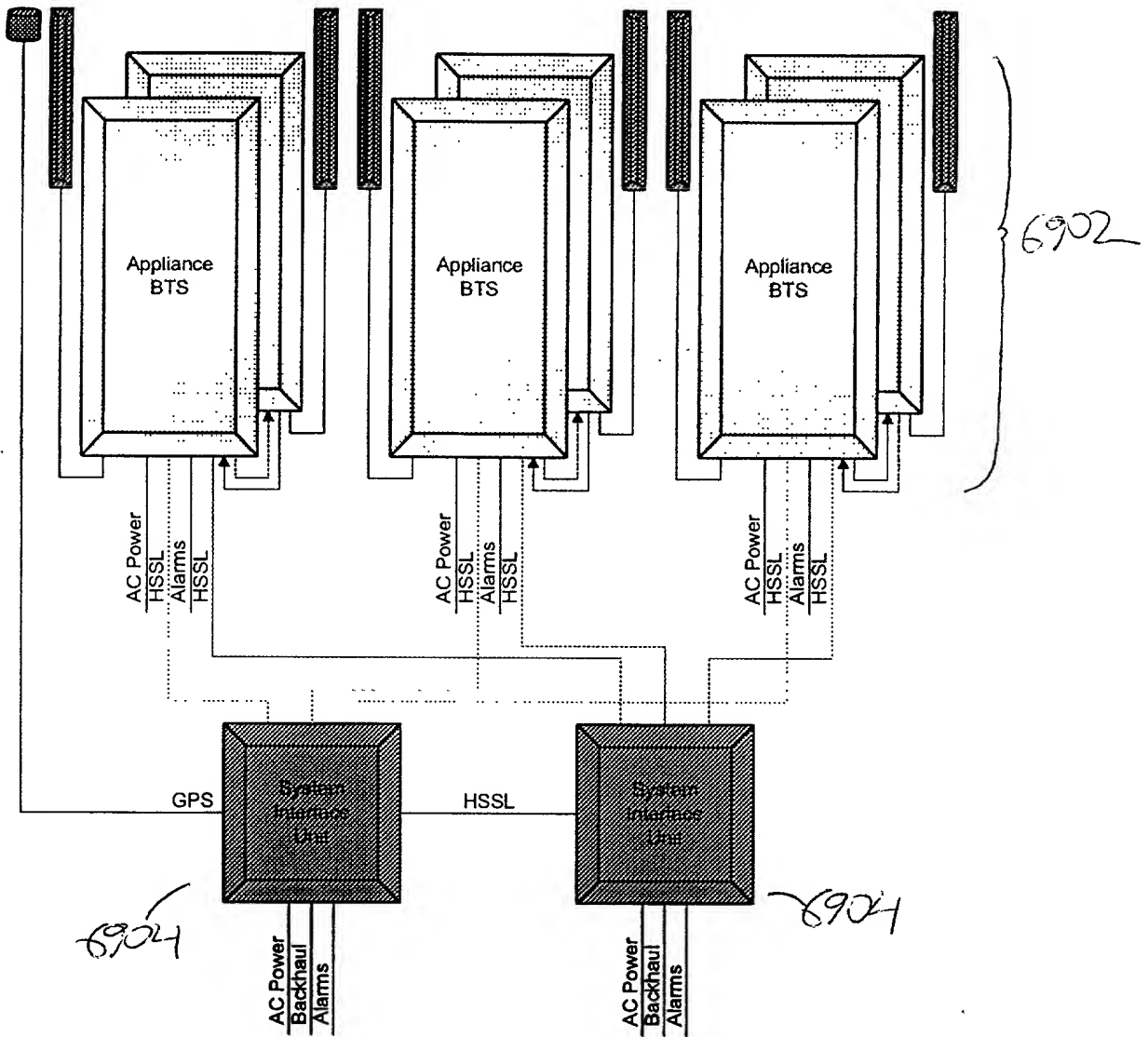


FIG. 69

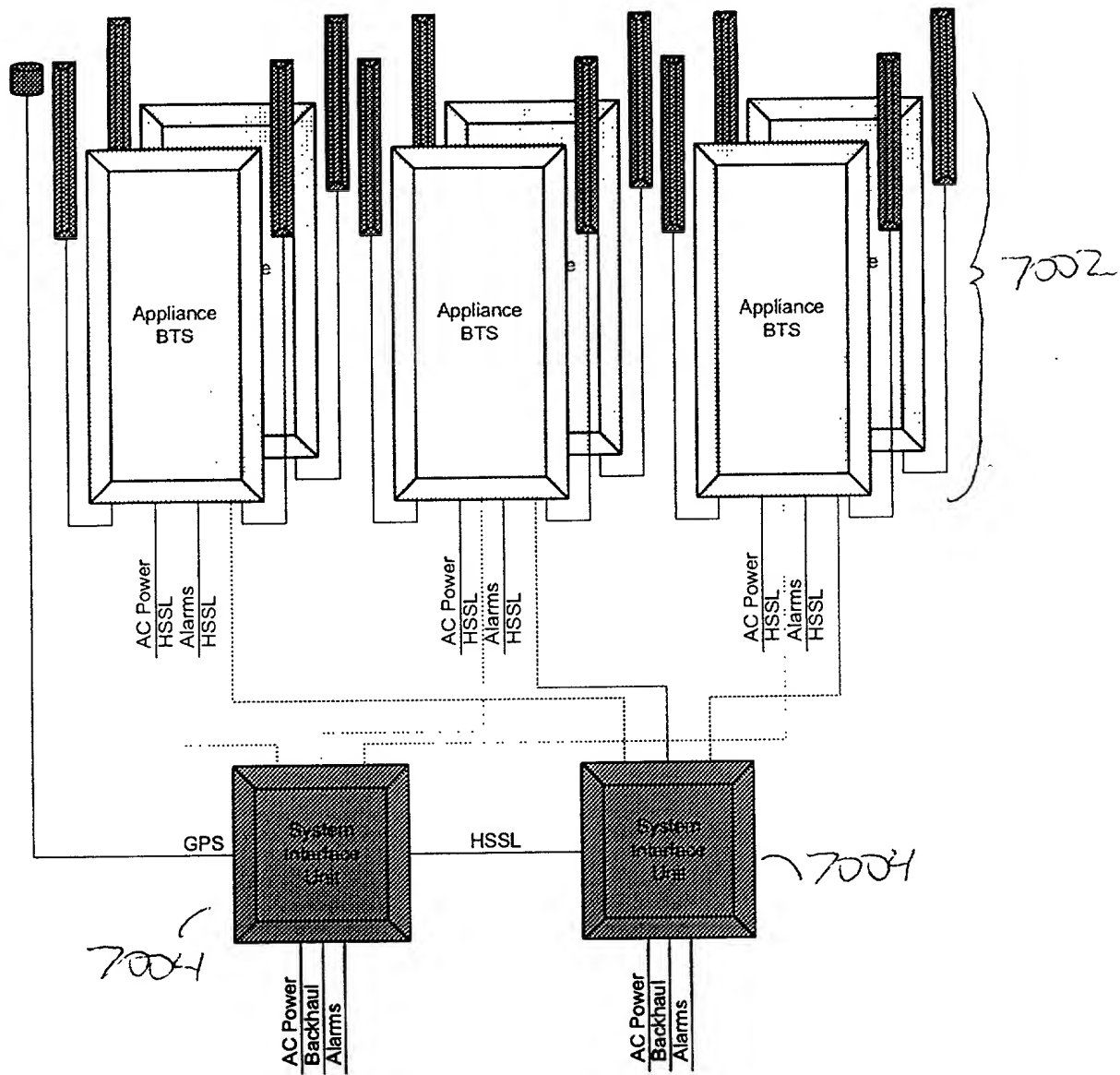


FIG. 70